What Designers Need to Know About USB Low-Power States

In addition to performance and interoperability, achieving low power has been one of the requirements for industry standards specifications. Some of the key specifications like Universal Serial Bus (USB), PCI Express (PCIe), and MIPI have defined power saving features for burst traffic. This whitepaper explains how Synopsys USB IP offers low power using various low power states that go beyond the basic features.

The USB 1.1 and USB 2.0 specifications support Suspend and Resume. Link Power Management (LPM) directed Suspend and fast Resume were added to USB 2.0 later. The USB 3.0 Super Speed specification supports U1 and U2 power states and U3 Suspend. All power states have seamless enter/exit while maintaining performance. U1, U2 and U3 states are also included in the USB 3.1 and USB 3.2 specifications. In USB4, the individual adapters maintain their respective low-power states, allowing the USB4 transport to enter the low-power CL1 or CL2 state during transfers and CLd state when the router enters sleep mode.

The Anatomy of a USB System

Before explaining the USB power management system, it is useful to review the anatomy of a USB system. A USB system consists of Host, Hubs, and Device components. The Host typically resides in computers or laptops or high-end handheld devices. The interface to Host is referred to as the Host Controller. Hub is a device that provides additional connectivity beyond the Host. Devices also known as peripherals provide useful functions, like human interface device (HID), mass storage, networking, audio headset, webcam, etc. The Host discovers connected devices, loads appropriate drivers, and links devices to their respective applications. The host schedules transfers between applications on the host and the useful function in USB devices.

Figure 1 illustrates a topology of how the Host, Hub and Device connect to form a USB system. Figure 2 shows a USB4 Host Controller system.
USB Power Management System

A centralized USB Power Management System could be a combination of software, hardware, and firmware implemented on Host. Power Management System communicates with a Host Controller through a set of programmable registers. A Host configures Devices through USB control transfers. During the process of enumerating Devices, the latency requirements to exit from the low-power states are communicated to a power management software. In turn, the power management software sets up Hosts and Devices for the desired power states by programming Host Controller registers. The power management software sets up Device settings through control transfers. In some implementations, parts of the power management tasks will be performed by the Hub driver on the Host System.

A logical representation of the USB power management system is illustrated in Figure 3.
USB Power States

In addition to the active power state during USB transfers, USB offers power-save states during idle. The power-save states define how each low power request is signaled, its handshake is confirmed, and the low-power state enters and exits such power-save states. The following section outlines how each power state is mapped and managed with respect to power saving functions, as illustrated in Figure 4.

USB 2.0 speed link supports L1 and L2 power states, USB 3.0 / 3.1 / 3.2 Enhanced Super Speed link supports U1, U2 and U3 power states. In addition to the U1, U2, and U3 power states, Synopsys USB IP also supports the proprietary U4 power state, which can be used when USB is not used. This reduces the idle power while waiting for an USB session to be established. Synopsys USB PHYs in the advanced process nodes also support the P4.PG power state where most of the PHY is power gated. Additionally, the USB Controller can also be power gated when USB is not used.

USB traffic is typically transferred in bursts. Figure 4 illustrates how the various power-save states in USB 2.0, 3.0, 3.1 and 3.2 are interleaved with active transfers.

Figure 4: USB Power saving states in USB 2.0 and USB 3.0/3.1/3.2

* Optional power save opportunity as implemented in the Synopsys USB IP
L2 state is initiated by the power management software on the Host system when it detects that transfers are inactive. The process starts with the Host Controller driver writing into the Host Controller register to suspend the port. In turn, the Host Controller stops all activities on the USB link including Start of Frame packets. The Device on the other end detects lack of any activity and after evaluating the timing of inactivity, the device enters the Suspend (L2) state.

L1 state, also known as Sleep state, is initiated by the Host downstream facing ports when the programmable L1 inactivity timer expires on the Host Controller. Alternatively, for a software initiated L1 power state, the power management software detects that the scheduled transfers are completed. In either case, the Host Controller sends Link Power Management (LPM) transaction indicating it wants to suspend the Device and how fast it can wake up and provide the service if requested. The Device decodes the transaction and after evaluating if the wakeup time meets its latency requirement, the device acknowledges the request. After this step, both Host and Device including PHY enters the L1 power state. USB Audio Device Class 3.0 specification extensively uses this feature. See References for further information.

Enhanced SuperSpeed U1 and U2 states are power saving states that can be entered if the link has been idle for some duration. U1 is used when USB is idle for tens of microseconds. U1 exit latency is in the order of few microseconds. U2 state is used when there are no scheduled transfers for hundreds of microseconds. U2 exit latency is also a few hundred microseconds. U1 and U2 are initiated by Host or Hub ports when the inactivity timers expire. For example, the process can start with Host Controller U1 inactivity timer expiring after a programmed threshold setting. In turn, the Host Controller sends Link Command indicating it wants to put the Device in the U1 low-power state. The Device evaluates the transfer states and data availability status, and optionally acknowledges the request. After this step Host and Device both enter the U1 state.

Note that request to enter U1 or U2 state can also be initiated by the Device when it detects no data transfers in progress. In the case of Hub Device, the U1/U2 request and acknowledgment to enter low-power state depends on the power states of Devices connected to the Hub Device. For example, the Hub cannot enter U1 or U2 state if connected devices are still in U0 (active) state since the hub blocks the traffic to the connected devices.

U3 Suspend state is initiated by the power management software when it detects no further transfers because the device is no longer actively used. A typical example is that web cam can be suspended when the video call has ended. The process starts with the Host Controller driver writing into the Host Controller register to suspend the port. In turn, Host Controller stops all activities on USB including Isochronous timestamp packets. Host Controller then sends Link Command indicating it wants to put the Device in the U3 low-power state. The Device on the other hand acknowledges the request. After this step Host and Device enter the U3 state. Host Controller and Device Controller then place their respective PHY to the lowest power state. The lowest power state in the PHY turns off the PLL and transmit/receive analog circuitry. This saves considerable power in the USB system.

The operating system can selectively suspend a device when no transfers are scheduled for the device. When all the devices are suspended, the Operating System can enter the sleep or hibernation state. In sleep or hibernation state, more power can be saved by power gating majority of the Host Controller, Device Controller, and PHY blocks, in addition to whatever else is not needed by the system to enter sleep or hibernation.

USB4 CL1 or CL2 is a low-power state with exit latency requirements of a few hundred microseconds. When the adapters are ready, USB4 logical layer initiates CL1 or CL2 state request. If the link partner is also ready for the requested low-power state, then the link partner acknowledges the request and then the logical layer enters the CL1 or CL2 state.

The power management software initiates the USB4 CLd state when it detects the transfers are not active anymore and will not be for quite some time. The process starts with connection manager software initiating USB4 router sleep state. USB4 router in response, after entering sleep state logical layer, is placed in the CLd state. CLd state can also be entered if there is a disconnect on the downstream port.

**The Anatomy of a USB Subsystem**

A typical USB subsystem has three major blocks: PHY layer, MAC (Media Access Control) layer and System Interface. This section describes how the various components of a USB subsystem interact during power saving functions.
The PHY block implements the required signaling on USB. It implements the data encoding/decoding as per the USB specification. It also interfaces to the MAC for data transmit/receive. The MAC block implements the protocol for the decoding/encoding of packets. It interfaces to the System for data transmit/receive across USB from/to the system memory. In USB4 Host controller, MAC can encompass all the adapters and their respective protocol controllers and the USB4 router. The intricate details of how each layer functions and their requirements are described in the USB specifications. The following sections describe how each layer functions with respect to power saving functions.

PHY contains PLL that generates USB subsystem clocks, and analog components for data transmission and receive, and signaling and detecting low-power states. In terms of power usage, the PHY consumes the largest portion of the USB subsystem power during active mode. The Host controller, which is a digital component for data path and control path consumes less power than the PHY. The system interface not including the other blocks of SoC will be the smallest power consuming component of the USB subsystem. However, note that system power which includes CPU (Central Processing Unit), memory and storage power can be significant, and typically much higher power than USB subsystem power. It is therefore vital that USB subsystem power save states are communicated through the subsystem to enable system power save states to reduce the total system power.

USB Subsystem Power Saving Features

USB defines two types of transfers: periodic transfers, and asynchronous transfers. Periodic transfers occur in bursts of packets within the given service interval. Asynchronous transfers occur in multiple bursts until a USB transfer is completed.

During periodic or asynchronous transfers, based on entry and exit latencies, USB allows the link to be placed in L1 or U1/U2 states for additional power savings. When scheduled transfers have completed, in other words when the application is not using the periodic or asynchronous endpoints anymore, USB is then placed in L2/U3 Suspend. An example of Suspend is when the video conferencing call ends and the webcam is no longer needed. Use of L1/U1/U2 and L2/U3 Suspend is illustrated in Figures 6 and 7.

The PHY block in the subsystem provides options to turn off the PLL or additional analog components depending on the power state it is placed in. This saves considerable power in the PHY during USB idle.

In addition to supporting these different PHY power states, the controller implementation can be optimized to enable additional power savings. The first option is to implement a clock gating scheme when fast exit latency is required to exit from low-power states. The second option is to implement a hibernation scheme where most of the controller is powered off. Both options are implemented in the Synopsys USB Controllers.

Figure 8 illustrates the mapping of clock gating and hibernation based on USB power states. For power L1/U1/U2 power states that have faster exit latency, power saving can be achieved by enabling clock gating. For L2/U3 power states, where the exit latency is high, power savings can be achieved by power gating different blocks.
Figure 8: Clock gating vs Hibernation state mapping of the USB states

Figure 9 illustrates a typical implementation of hibernation scheme. It consists of a small block that is always powered to monitor for USB events. The rest of the Controller can be power gated after storing controller state in always-on memory. When a USB event is detected, the powered USB block generates power restore request. The controller state is restored from always-on memory, and controller becomes operational again allowing data transfers to continue. In USB4 Host or Device, different protocol controllers can hibernate based on their local link state. The entire USB4 Host or Device can hibernate when the router enters sleep state or disconnects.

Figure 9: A typical hibernation scheme implementation

Conclusion

USB defines many power saving states as described in this paper. The Synopsys USB IP portfolio consists of USB IP for Host, Device and Dual role Device supporting all USB speeds from USB 2.0 to USB 3.2 and USB PHYs from USB 2.0 to USB4. Synopsys USB Controllers and PHYs support enhanced methods for power savings during the USB-protocol-defined low-power states. The controller and PHY documentation provide the hardware and software programming interface details for control of such power features. Synopsys USB Controllers and PHYs are certified by independent test labs (ITL) approved by the USB-IF. SoC integrators can use these certified controllers and PHYs as building blocks to expedite their development of power efficient SoCs.

References

Universal Serial Bus 2.0 Specification
Universal Serial Bus 3.2 Specification
Universal Serial Bus 4 Specification