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WHITE PAPER

Achieving Your Low Power Goals with Synopsys Ultra Low Leakage IO

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Introduction

The demand for low power design has intensified with shrinking geometries. At the same time, innovation in battery operated, handheld devices has increased the design complexity by adding more and more functionality. The focus is on power-optimized designs while maintaining low cost and reduced risk. Designers face these complex and contradictory challenges: developing products with the lowest possible power consumption, maintaining high performance, integrating new connectivity standards, and moving to the smallest process technologies while keeping costs down.

Optimizing the power helps extend battery life, one of the most critical requirements in consumer and mobile applications. General Purpose IOs (GPIOs) are an essential block in a system-on-chip (SoC). GPIOs are the standard chip interface that communicates between on-chip logic operating at low voltages and off-chip components operating at similar or higher voltages. As functionality is added to the SoC, the number of pin connections to the external interfaces increases, and therefore the number of GPIOs needed in the SoC increases. With so many GPIOs in a design, it is critical to ensure they consume as little leakage power as possible to minimize the impact on the overall leakage at the SoC level while maintaining high frequencies of 100s of MHz for proper IO operation.

Leakage is often considered a device artifact that cannot be avoided, however, experienced IP designers adopt different design techniques to reduce leakage in the IOs. One example is to use Foundry-provided Ultra Low Leakage (ULL) Metal Oxide Semiconductor (MOS) devices. Unfortunately, because these MOS devices have higher threshold voltages, which reduce the device performance and circuit performance, they are of limited use. Therefore, designing the circuits to alleviate any leakage paths in the design is critical.

This whitepaper explains the need for ULL GPIOs, the optimization techniques used to reduce leakage, and the inherent tradeoffs to consider. Finally, it describes how Synopsys ULL GPIOs help designers reduce leakage while achieving the SoC power and performance targets for mobile and battery-driven devices used in AI and sensing applications.

Need for ULL GPIOs

Leakage is increasing exponentially with each technology generation. Device threshold voltage scaling, shrinking device dimensions, and larger circuit sizes are causing this dramatic increase in leakage. Some industry experts believe it will one day become the dominant portion of the total power consumed by SoCs. As leakage grows with evolving process parameters, it often impacts wafer yield and power constrained SoCs. Traditionally, leakage has been considered an important design variable in handheld devices and for standby circuit operation. However, the significant increase in the contribution of leakage power to the total power of a design now makes leakage a critical design variable in all SoC designs, and IO libraries must address the need for ultra-low-leakage solutions.

The SoC must support several functionalities. These functionalities are managed by various input signals connected via the GPIOs to the digital core or the analog IP inside the SoC. There are often large numbers of GPIOs in the padring of an SoC, so the leakage of a given GPIO is multiplied by the number of instances of that GPIO in the padring. Therefore, designers should look for any opportunity to reduce the leakage of a GPIO. Furthermore, operating at very low supply voltages is necessary for smaller device sizes and aggressive voltage scaling. Still, it increases leakage power proportionally to the threshold limit in the devices supporting those lower voltage supplies, reinforcing the need for an ultra-low-leakage solution.

Another consideration is the power-rail electrostatic discharge (ESD) clamp circuit, which is essential in on-chip ESD protection design and a critical part of GPIOs. ESD components with a large MOS capacitor in the ESD detection circuit will cause massive leakage under power-on conditions. Because of this impact, ESD leakage must be carefully monitored, even for ULL GPIOs.

In an SoC, the IOs generally contribute about 10% of the total leakage power (Figure 1). ULL GPIOs differentiate from their non-ULL counterparts because of their standby leakage, which can be 100 times lower than those in non-ULL GPIOs. Designers can successfully achieve their leakage and low-power targets by using ULL GPIOs in designs for small battery-driven devices used in AI and sensing applications. And since these applications are not generally pushing performance, the lower performance of the ULL GPIOs is not a concern.

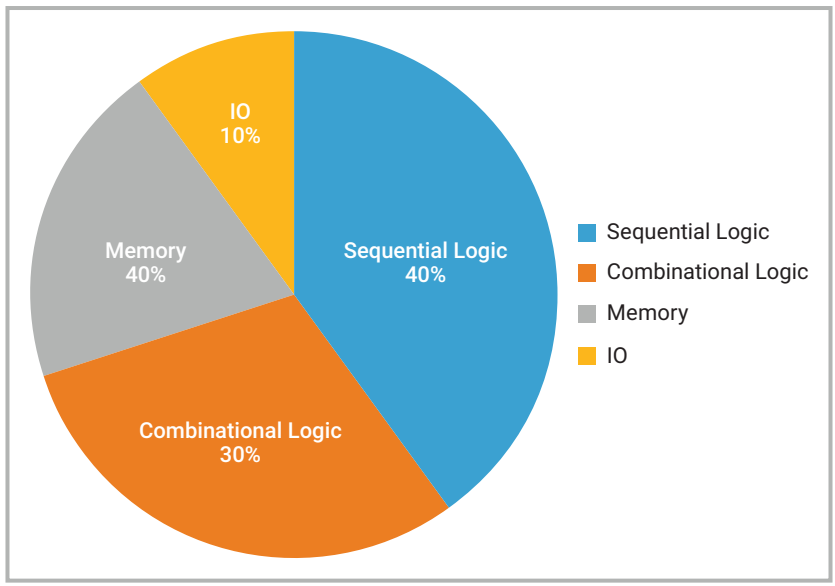

Figure 1: Power distribution in microprocessors [1]

Leakage Optimization Techniques

Specific optimization techniques at the transistor level and the circuit level have demonstrated effective leakage reduction:

- At the transistor level, increasing the length of the devices helps reduce leakage. Lower voltage threshold (Vt) devices or thin gate devices are used when the voltage supply range is very low or there is a need to support a higher frequency of operation, but they consume more leakage power. For higher supply ranges, thick gates or higher Vt devices are used.
- Some fully depleted silicon-on-insulator (FDSOI) technologies, offering several types of devices such as Silicon-on-thin BOX (SOTB), have demonstrated very low standby leakage. Adaptive reverse body biasing techniques in FDSOI technologies have also helped dynamically control standby leakage by changing body bias while maintaining performance.
- At the circuit level, leakage optimization involves removing high leakage current paths by eliminating DC paths in the circuits.
  - Power gating enables devices to be switched off when unnecessary, reducing the gate-induced drain and reverse bias leakage power. Using tri-state inverters instead of transmission gates has shown even better leakage performance.
  - Device stacking is used to control leakage for technology nodes with very low fixed transistor lengths. The leakage of a two-transistor stack is approximately an order of magnitude less than that of a single transistor, as shown in Figure 2.

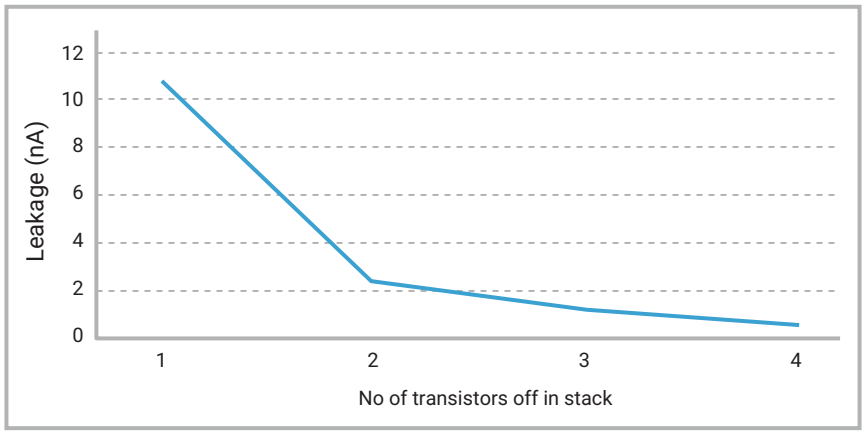

Figure 2: Subthreshold leakage current in different stacks of off-transistors [1]

Figure 3 shows lab results from Synopsys ULL GPIO development designs for different IO supply mode operations. This was done on a digital "supply-to-interface-supply" level shifter 'circuit' while employing various leakage optimization techniques and measuring the leakage reduction seen with each technique. By combining these techniques, we can achieve significant leakage reduction on a level shifter which, when employed in a GPIO design, will help reduce the overall GPIO leakage power.

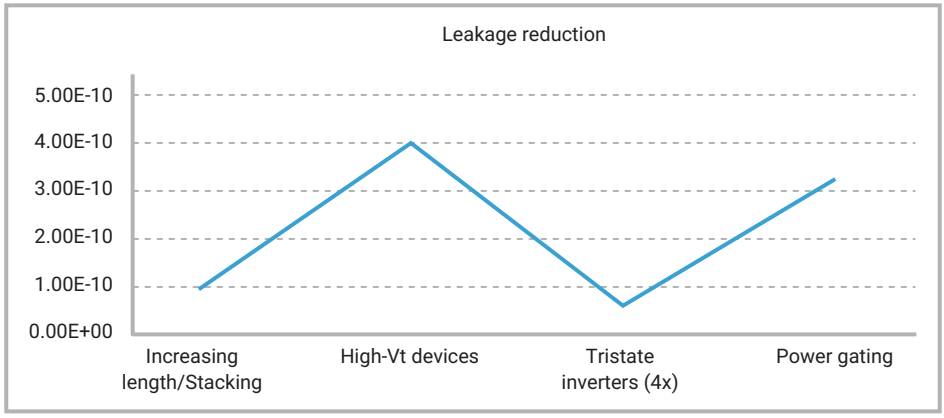

Figure 3: Leakage reduction with optimization techniques—digital supply level shifter circuit on GPIO (Source: Synopsys)

Tradeoffs for ULL GPIO Designs

Adopting ultra-low leakage in low-power designs comes with performance, power, and area tradeoffs. When designing with ULL GPIOs, SoC designers should be aware of the following:

- The use of thick-gate oxide devices or high-Vt devices comes at the cost of reduced performance in terms of operating frequency.
- An increase in gate length reduces leakage but increases cell area, and the width must grow in the same proportion to maintain performance, which further impacts the area.
- Unconventional ULL techniques, e.g., the nMOS transistor implementation, make the circuit complex and may have limited practical applications.
- SOTB devices and ABB techniques lead to higher mask costs, added circuit complexities, and area overhead.
- Power-gating leads to high-z nodes which can cause unwanted glitches, especially during power sequencing scenarios.

Synopsys ULL GPIO offerings

Synopsys offers multiple varieties of GPIOs supporting ultra-low leakage for a wide range of voltage supplies from 1.2V to 3.3V. Synopsys Ultra Low Leakage GPIOs adopt device and circuit optimization techniques, along with additional advanced techniques such as power-gating, optimization of static and data paths, and use of appropriate devices based on threshold voltage and leakage profile. Using special MOS field-effect transistors (FETs), such as extended diffusion-based devices, has helped reduce leakage while still achieving good performance. The Synopsys ULL GPIOs are rich in features while maintaining ultra-low leakage requirements. Some of the key features include:

- Ultra-low leakage
- Operating frequency of up to 50MHz
- Programmable output drive current options
- Selectable output slew rate
- Programmable input Schmitt trigger
- Programmable input options such as bus-hold, weak pull-up/down, and retention
- No electrical over-stress or aging issues, even with 2XVDD operation using VDD tolerant devices
- Support for fail-safe functionality, ensuring low leakage through the pad in the absence of supply

Figure 4 shows a block diagram with the major components of a GPIO. Tx and Rx have level shifters, which are needed to scale the signal voltage up or down for both the data and control paths. The control level shifters have inputs that are primarily static signals and can be optimized for leakage over performance by reducing the sizes of the devices and using devices that inherently have low leakage and high Vt.

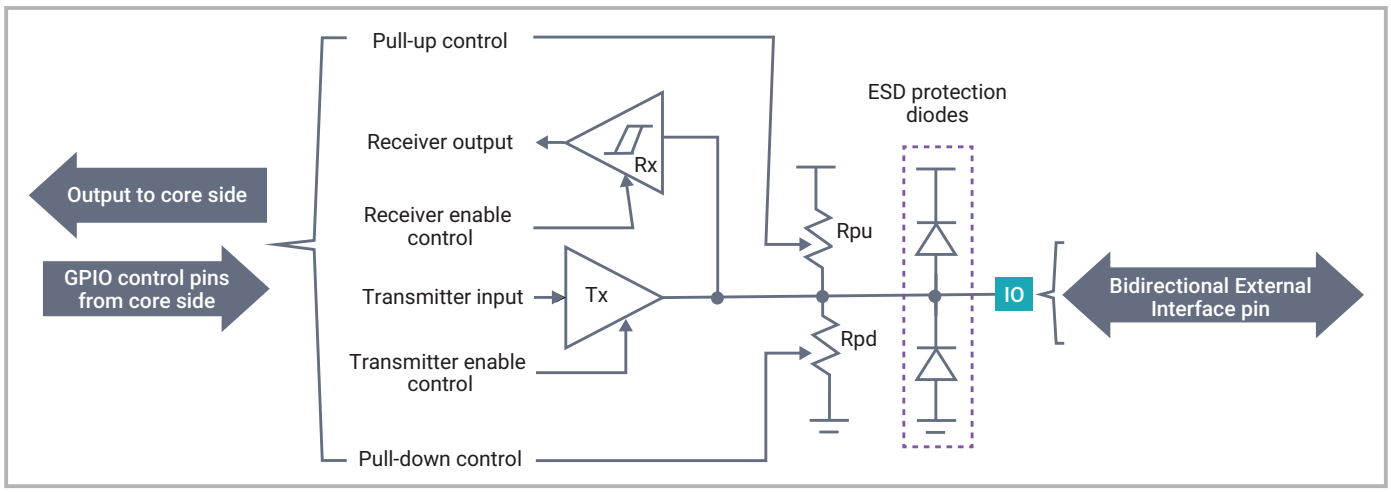

Figure 4: Main components and signals of the GPIOs [2]

The frequency of data signals is on the order of MHz, and the data level shifter must support this frequency. By power gating and proper safe stating of the data generator, Synopsys ULL GPIO limits the block's leakage. However, power gating has its limitations, as it can impact the gated node voltages during power sequencing, leading to unwanted glitches on the pad outputs. In this case, Synopsys ULL GPIO ensures no high current glitches are present. Tristate inverters are preferred over transmission gates because they show better performance in controlling leakage.

Synopsys GPIOs utilize leakage optimization techniques where the IO supply is equal to the tolerance limit of the devices. However, designing IO which operates at high voltage using lower voltage tolerant devices is necessary, which can impact the circuit's reliability. To address such concerns, Synopsys provides a reference generator block with a very low leakage current, along with the ULL GPIO offerings.

Conclusion

Ultra-low leakage GPIOs are essential components in most SoC applications where power is a critical design attribute. The padring at the SoC periphery has many GPIO cells, and each cell must have the lowest leakage possible. However, leakage optimization techniques can negatively impact performance, area, and circuit complexities, so these techniques must be used judiciously in GPIO design. The GPIOs must maintain low leakage and meet performance requirements, with some frequency requirements in the order of MHz. The control path and data path can be optimized independently, and power gating can also be employed to remove leakage paths. Leakage optimization can be performed at both the circuit level, through various architectural techniques, and at the device level, by using multiple voltage threshold devices in the GPIOs.

Synopsys' IO portfolio includes a wide variety of robust GPIOs and specialty IOs (LVDS, SD/eMMC, I2C, and I3C), helping designers achieve power, performance, and area (PPA) targets for their SoCs, with low risk and fast time-to-market. For more information, visit Synopsys I/O library IP.

References

[1] Leakage Current in Sub-Micrometer CMOS Gates by Paulo Francisco Butzen and Renato Perez Ribas

[2] GPIOs: Critical IP for Automotive Functional Safety Applications by Nidhi Bhasin, Shivakumar Chonnad, Vladimir Litovtchecnko and Sowjanya Syamala

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