SIGNAL INTEGRITY

& Simulation Considerations in Backplane Designs for Military Systems

an Elma White Paper

ELMA

Your Solution Partner

www.elma.com

Electrical interfaces and connectors today face signal integrity challenges which weren't a real concern 15 or even 10 years ago. This is especially true for military systems such as radar, electronic warfare, and signals intelligence (SIGINT) that continue to grow in complexity to fulfill the ever-increasing demand for improved intelligence, surveillance, and reconnaissance (ISR) data.

As the signal density for connectors continues to get tighter and footprints get smaller, problems like crosstalk and the geometry of the launch into/out of the connector pins start to play a major role in the performance of backplane channels. Regardless of the backplane topology, signal integrity analysis follows the same procedure: pre-layout analysis, post-layout analysis, measurements, and correlations between simulations and measurements.

This white paper addresses the following:

- How to properly perform signal integrity analysis of connectors and backplanes
- How to leverage simulation techniques to ease this procedure and reduce costs in the long run
- How to measure the performance of backplane links

Signal Integrity Concerns

Signal integrity doesn't care how connectors are labeled or what the industry calls them; it only cares about what the signal sees in its path. The same holds true for the system, which supports signal propagation through various media. Multiboard systems (such as backplane-based systems) see the signal traveling through mated interface connectors and PCB traces. These spots are precisely where signal integrity must be maintained. The same principles, methodology, and concerns are also raised in many other systems, whether based on ATCA, CompactPCI-Serial, PCI Express (such as in-PC motherboards that use the PCI Express connectors), or entirely custom.

For this paper, we will use the VPX standard (VITA 46) to illustrate our points. VPX is a defined system architecture based on VITA 48 mechanical packaging requirements. The VPX standard is written in terms of rules, permissions, and observations. Specifically, the VPX standard initially defined the use of a new connector called the MultiGig RT2™; additional connectors having the same mechanical and similar electrical characteristics have subsequently been recognized.

A Little History: VITA Backplanes and Connectors

Backplane connectors have come a long way since the introduction of the first VME bus connectors more than thirty years ago. These connectors were based on a 0.1" grid; crosstalk within mated connector interfaces, return loss at the vias of the connector's footprint, and impedance discontinuities of +/-20 percent weren't topics of concern at the data rates that these parallel multi-drop architectures were transmitting.

Fast forward a few decades after VME's birth: VITA pushed forth the VPX standard to meet the higher performance and increased reliability requirements of military and aerospace systems. Designed from the ground up, VITA came up with VPX, or VITA 46.0, to implement modern high-speed serial interconnects, real-time monitoring, and mitigation of certain system parameters in harsh environmental applications.

Following the promulgation of VPX, Elma and other defense electronics suppliers within VITA introduced OpenVPX (VITA 65) to address many of the interoperability and configuration concerns with VPX. The OpenVPX initiative defines clear interoperability points necessary for integration between module-to-module, module-to-backplane, and chassis. For each enumerated rule within VITA 65 a compliance method was defined.

The Connector Challenge Today

Data density was quite low 25 to 30 years ago. Today, however, high-density connectors are boasting data rates that approach what is

practically feasible over copper — 25 to 28 gigabits per second. The VPX connector, while initially intended to support 8 and 10 Gigabaud signaling, has recently been redesigned to support signaling at 16 and 25 Gigabaud. Implementing a backplane connector system needs to be a precise and methodical process to ensure they can perform properly and enable signal integrity in military systems. See Figure 1 below.

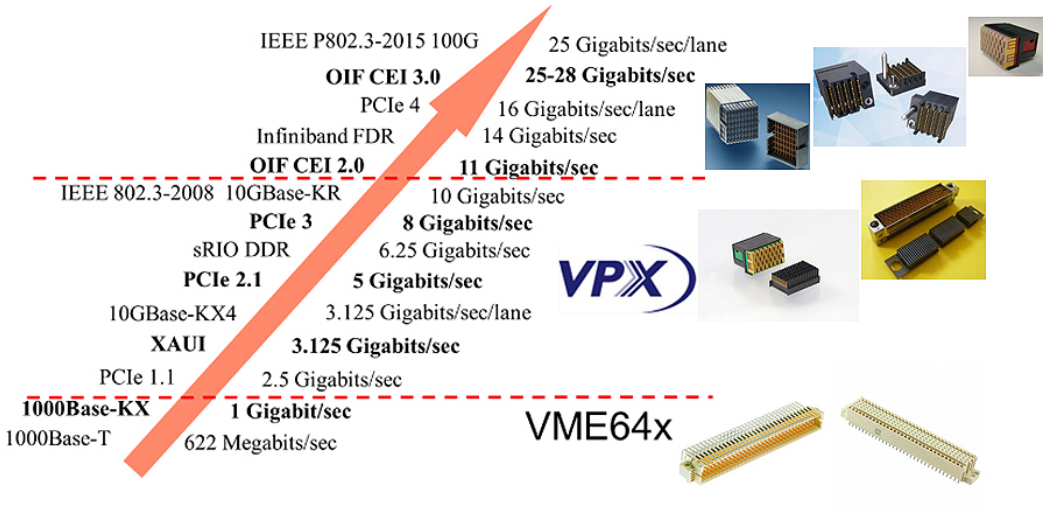


Figure 1: Advances and challenges in connector technology and standardization.

Channel analysis starts with evaluation of the models of the building blocks that make up the channel. For instance, the electrical models provided by the connector manufacturers need to be evaluated for the application. The frequency over which the model performs and the step value must be sufficient for the fastest signals in a given backplane design. In addition, it is the responsibility of the signal integrity engineer to ensure that the following aspects of the design are addressed:

- their models are checked for passivity and causality (as different manufacturers use different methods of extracting a mated interface multi-line S-parameter model).
- their behavior is observed when they're part of different channels having different parameters (different lengths, different topology, different geometry, etc.); performance needs to be monitored, as it becomes less predictable at higher data rates and even more so at data rates for which the parts weren't designed.
- their footprints are properly designed, both on the backplane and daughtercard, to facilitate the higher data transmission rates. Typically, connector manufacturers would recommend pad/antipad/trace geometries, but in many cases these aren't optimized.

Signal Integrity Analysis

It is essential that designers compare the data from the connectors and PCB manufacturers with the experimental results when doing pre- and post-layout signal integrity analysis of channels.

Typically concatenation (or cascading) of S-parameters is the practical method of choice to do pre- and post-layout signal integrity analysis of a channel. However, some important aspects which are often overlooked are:

- At higher data rates, the behavior of a complete channel is NOT the sum of the behaviors of its individual subsections (or as Aristotle put it more than 2,300 years ago, "The totality is not, as it were, a mere heap, but the whole is something besides the parts.").

- Cascading is built on the assumption that there are no non-transverse electromagnetic (non-TEM) interactions occurring at the interface between the connector and its footprints.
- While S-parameters are useful for measurements and describing network response, they are not as useful for network embedding and de-embedding. To perform these operations other network parameters are better suited, either T-parameters or ABCD matrix[i].

With T-parameters, we can perform matrix multiplication for the cascading networks operations to get the total network T-parameters and transform back to S-parameters. These formulas assume that the Z0 impedance is purely real and the same on both sides of the S-parameter test setup[i].

The condition to be able to cascade/multiply S/T parameters is that all models are normalized to the same impedance and that the characteristic impedance of the segments is the same and equal to that of the system.

Unfortunately, the overall transfer function of a highly cascaded system equals the product of the s21 transmission coefficients if and only if the reflections are all negligible . The S-parameter cascading method requires that the measurements be made at some particular impedance (Z0). For best results, this impedance should be reasonably close to the impedance under which your circuit element will actually operate[ii].

Optimizing Backplane Links Takes Teamwork

Most high-speed systems route multiple links to the backplane via connectors and daughtercards. Each link in a backplane-based system contributes in its own unique way to the performance of the overall system, as each will potentially affect the performance of otherwise good links and could cause bottlenecks in the bandwidth of the entire system through excessive crosstalk.

All these links must work together or the system will fail. For example, let's say that the designer of one of the system cards starts with a relatively low loss dielectric, but because of the way some of the links were routed, the maximum performance of certain links can't be achieved.

Through co-design – that is, cooperation at the layout stage (developing the backplane in parallel with the daughtercards) and having feedback circulated between the design teams – the performance of the links in this engineer's design was optimized, yielding a better return loss but,

"All these links must work together or the system will fail."

more importantly, a much better insertion loss deviation, which in turn results in a much better margin.

Typical examples of improvements in the layout would include:

- the routing to and around the DC blocking capacitors near transceivers
- changing the dielectric material (even if only on the high-speed layers)
- optimizing the antipad shape and size for the vias that carry high-speed signals
- specifying the type of weave to be used on the layers that carry high-speed signals.

The best way to ensure signal integrity from every link is to create accurate models, perform proper pre-layout simulation and evaluate the result with

first article measurements. Such efforts at the beginning of a design will save countless work hours and costs that would be incurred by having to reengineer the whole design or – worse yet – delivering a solution with poor signal integrity. See Figure 2.

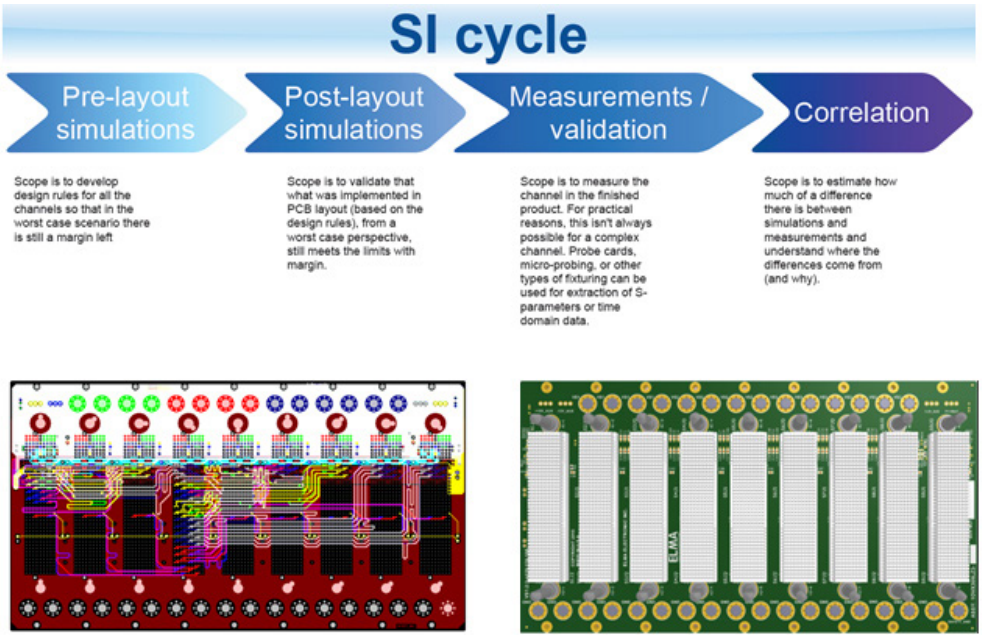


Figure 2: *Signal integrity flow in channel design*

Simulation

A pre-layout simulation can only be as good as the models and assumptions that are being used in the process. Different simulations also create different assumptions. The further from reality the models and assumptions are, the less correlation everything will have with measurements – provided the measurements are done accurately, of course.

For example, in most simulations, the following assumptions are routinely made:

a) the dielectric material surrounding the traces in the backplane or daughtercard PCBs is assumed to be homogenous and isotropic in all directions. Furthermore, one has to choose a particular model for the behavior of the dielectric constant over the frequency range of interest (Debye, Djordjevic-Sarkar, etc.)

b) the copper foil roughness and resistivity is assumed to follow a certain profile/model or another; while in reality processed laminates can have varying degrees of roughness on the same foil, depending on the ability of the PCB manufacturer to employ this method. Typical models include the Huray snowball model, Hammerstad, etc.

c) the ports of the models, which technically represent the points at which the cascading occurs, are ideal wave ports or ideal lumped ports ideally placed at points where there is only TEM propagation

d) effect of the compliant pin inside the via barrel is negligible

e) all other lines/aggressors are terminated with perfect impedance match

VPX Probe Card

As mentioned at the beginning of this paper, signal integrity analysis follows the same procedure: model creation and validation, pre-layout analysis, post-layout analysis, measurements and correlations between simulations and measurements – regardless of backplane topology. Each stage may require specific expertise as well as collaboration between different persons to achieve the stated goals in a time-efficient and cost-effective manner.

Testing such solutions for signal integrity requires versatility to measure the different parameters of backplanes, regardless of standard.

Elma worked with a signal integrity company to develop a pair of test fixtures for VPX backplanes, which were named VPX Probe Cards. These fixtures are flexible and can be used to measure the performance of any links within the backplane using parameters such as differential return loss, differential insertion loss, and crosstalk – if and only if the loss introduced by it can be accurately and completely characterized. See Figure 3 below.

Today's high-speed VPX systems require extremely accurate channel characterization analysis in order to ensure optimal system-level performance in critical applications. The amount of loss on the VPX probe card can and should be de-embedded from the total channel measurements by measuring the corresponding structure on the calibration card, or through other methods such as automatic fixture removal (AFR) if one is using Keysight's ADS/PLTS platform, or in-situ de-embedding, or one of a host of other techniques.

The VPX probe card is kept securely in place by a patented mechanical support/fixture, which makes it easy to move the card to the desired position even while multiple VNA cables are attached to it.

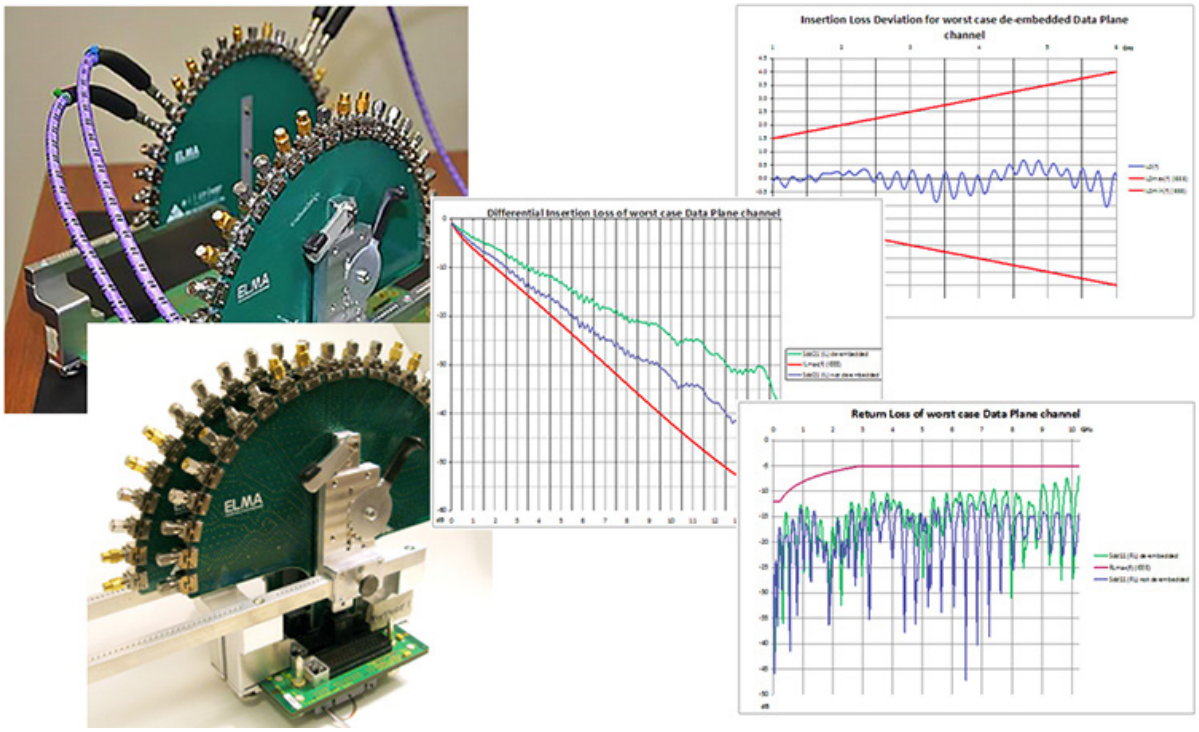


Figure 3: *Backplane channel measurement tools and sample test data show the necessity of good launches.*

Additional parameters such as insertion loss deviation, fitted attenuation, insertion loss to crosstalk ratio, or channel operating margin (as defined in IEEE 802.3-2015) can be computed from the measured parameters with suitable computation platforms.

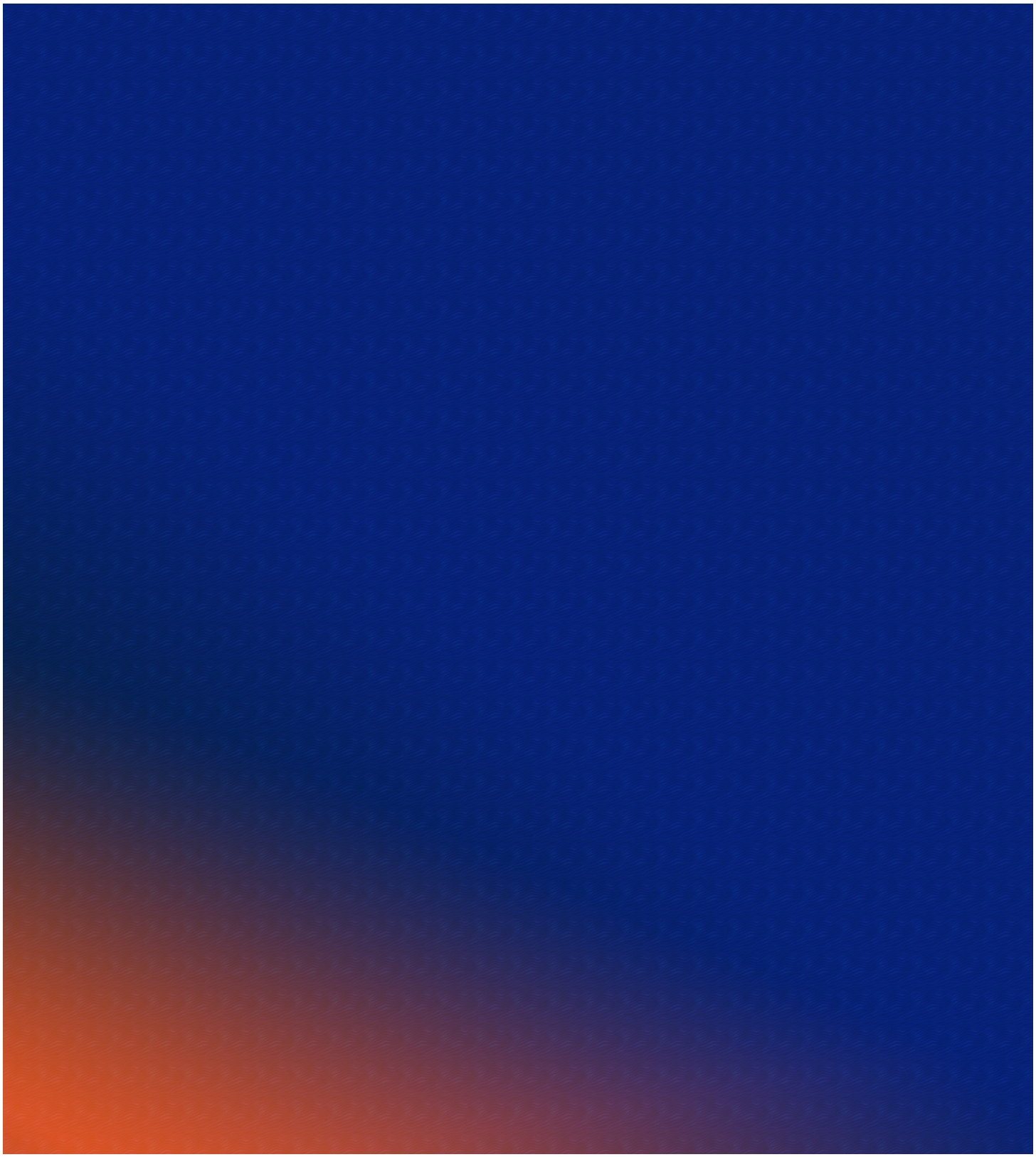
Elma's Backplane Probe Cards enable the characterization of differential VPX backplane channels between any two points on any 3U or 6U VPX backplane. It's designed for use on backplanes intended to support PCIe 2.1 (5.0 Gbps), Infiniband DDR (5.0 Gbps), Serial Rapid IO 2.2 (6.25 Gbps), PCIe 3.0 (8Gbps), Ethernet 10GBASE-KR (10Gbps), Infiniband QDR (10 Gbps), or Infiniband FDR (14.4 Gbps) signaling.

Conclusion

Connector technology will only become more complex as the demand for greater data density increases. Ensuring signal integrity with every backplane link – where the signal travels through mated interface connectors and PCB traces – is essential.

No matter the backplane topology – VPX, CompactPCI, ATCA, etc. – the same principles, methodology, and concerns will apply. Integrating testing fixtures such as the VPX Probe Cards and working with the connector manufacturers to leverage proper simulation and modeling techniques – pre- and post-layout – will ensure signal integrity, cut down on errors in design, and reduce costs in the long run.

For more information on Elma's embedded technology, including the VPX Probe Card, visit www.elma.com.



ELMA

Your Solution Partner

www.elma.com