Putting VPX and OpenVPX to Work

By: Rodger H. Hosking

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Setting the Standard for Digital Signal Processing

Putting VPX and OpenVPX to Work

Second Edition

VPX, VPX REDI, OpenVPX

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by

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Preface

Before the advent of OpenVPX, designers of embedded systems took advantage of the extreme connectivity offered by VPX (VITA 46), but were faced with a virtually unlimited number of possible implementations. Specific choices for the control and data channel assignments for each slot, the backplane connectivity, and serial fabrics were often made somewhat arbitrarily to suit the particular needs of the current system. Although following the general framework of VITA 46, each system tended to be so unique, that the boards and backplanes designed for one system were seldom usable in other systems, even from the same vendor.

Now, OpenVPX provides an effective method for describing VPX components, and also defines numerous "profiles" for boards, slots and backplanes that detail specific configurations of channels, interconnections and fabrics. Instead of starting from scratch each time, designers can browse through these standardized profiles to find one that satisfies the objectives of each new system.

By narrowing the field of configurations, these profiles boost reusability and interoperability between vendors. OpenVPX presents a formal, well-organized system for defining all components in VPX systems, and the efforts of the working group should be applauded. Many of the figures and the profiles in this handbook were derived from the full OpenVPX specification. The OpenVPX specification is maintained by VITA as VITA 65.

For more information on complementary subjects, the reader is referred to these Pentek Handbooks:

Critical Techniques for High-Speed A/D Converters in Real-Time Systems

High-Speed Switched Serial Fabrics Improve System Design

Putting FPGAs to Work in Software Radio Systems

High-Speed, Real-Time Recording Systems

Software-Defined Radio

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VPX, VPX REDI, OpenVPX

VPX

- Switched Fabric Links Boost I/O Speed
  - Eliminates parallel bus backplane bottlenecks
  - 8 to 24 gigabit serial 4X links for each card slot
- Optional Switch Card
  - Programmable reconfiguration of serial link connectors
- 3U and 6U Form Factors
  - Same dimensions as VME
- New Backplane I/O Options
  - Optical and RF backplanes now available
- Fully Compliant With XMC Modules
  - VITA 42 XMC specification
- Modernized Power Distribution
  - Supports high-power and high-density cards

Figure 1

VPX REDI

- REDI - Ruggedized Enhanced Design Implementation
- Defines Specific Mechanical Design Implementations for VPX
- Enhanced thermal management
  - Air, conduction, and liquid cooling
- Improved structural integrity
  - Cover plates to protect circuitry and ESD protection
- 2 Level Maintenance compatibility
  - Modules can be field swapped for field maintenance
- Dot Specifications Define Implementation Details
  - VITA 48.1 – REDI Air Cooling
  - VITA 48.2 – REDI Conduction Cooling
  - VITA 48.3 – REDI Liquid Cooling
  - VITA 48.5 – Air Flow Through Cooling

Figure 2

To eliminate backplane bottlenecks of the venerable VME architecture, the embedded community launched the VPX initiative, formally defined under VITA 46.

The shared, parallel VMEbus connecting all card slots is completely replaced by numerous point-to-point gigabit serial links between VPX card slots.

VPX shares the same outline as 3U and 6U cards and supports XMC mezzanine modules defined under the VITA 42 standard.

VPX uses three MultiGig RT connectors for a 3U card and seven for a 6U card.

As a result, VPX cards boost the traffic bandwidth by a several orders of magnitude compared to VME.

The VITA 46.0 VPX base specification does not define backplane topologies or specific gigabit serial fabrics or protocols.

Implementations of each fabric protocol are defined as subspecifications, or “dot specs.”

VPX™

As industry started using VPX, a new extension emerged to deal with severe environmental requirements.

The VITA 48 REDI (Ruggedized Enhanced Design Implementation) defines specific mechanical designs for enhanced thermal management using forced air, conduction cooling, and liquid cooling methods.

It also defines protective metal covers for the cards to satisfy new requirements for simplified field servicing in deployed military applications.

VPX REDI

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VPX, VPX REDI, OpenVPX

OpenVPX Initiative

- Rationale
  - To embrace VPX as a new system architecture, U.S. DOD mandated industry-wide definition and adoption of standards for VPX technology
  - Provide interoperability across vendors
  - Promote market priced components among competitors
  - Provide long-term availability for life-cycle support
- OpenVPX Industry Organization was formed in January 2009
  - 26 embedded system vendors, manufacturers and contractors
  - Goal: accelerate definition and turn over to VITA for standardization
- Transition to VITA Standard
  - Transferred to VSO (VITA Standards Organization) in October 2009
  - Designated as VITA 65
  - Ratified by VITA in February 2010
- ANSI Standardization
  - Received in June 2010

Figure 3

OpenVPX: VITA 65

- Defines sets of system implementations and system architectures
  - Promotes multi-vendor interoperability and life-cycle maintenance
  - Uses existing VITA 46 VPX Baseline and VITA 48 VPX REDI standards
- Defines various sizes of ***pipes*** used for serial communication
- Defines various ***profiles*** for structure and hierarchy:
  - slot profiles
  - backplane profiles
  - module profiles
  - development chassis profile
- Defines multiple ***planes*** for signal types within the specification:
  - Utility
  - Management
  - Control
  - Data
  - Expansion

Figure 4

The OpenVPX organization was formed in January 2009 to promote industry-wide standards and long-term availability of VPX technology across the industry. The original VPX specification was being used, but because it permitted such a wide range of architectures, VPX systems tended to be unique, vendor-specific implementations.

The mission of OpenVPX was to enhance the original VPX standard by adding a set of well-defined system architectures, nomenclature and conventions to enable interoperability among vendors. Consisting of key vendors in the embedded-system community, all eager to convince government and military customers that VPX was suitable for current and future systems, the group made fast progress and turned over the completed specification to the VSO in October 2009 for standardization under VITA 65. In February 2010, the specification was ratified by VSO and ANSI approval was received in June 2010.

OpenVPX™

OpenVPX defined new nomenclature for systems to describe the gigabit serial links in terms of the number of lanes and their function. The term “pipe” is used to define the number of bidirectional differential serial pairs that are grouped together to form a logical data channel.

OpenVPX also categorized the different kinds of traffic carried though the pipes as “planes”. The five planes defined are the utility, management, control, data, and expansion planes.

In order to define architectural characteristics of systems, several “profiles” were defined. A slot profile specifies the pipes and planes found on the backplane connectors of each slot. The module profile specifies the pipes, planes, fabrics and protocols implemented on each card. The backplane profile defines how the slots are connected to each other by pipes. And finally, the development chassis profile includes the backplane profile and defines the dimensions, power supply, and cooling method.

VPX, VPX REDI, OpenVPX

3U VPX Board

- 3U board outline same as 3U VME
- P0 Utility Connector
  - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT-2 for P1 and P2 Signal Connectors
  - Definitions for differential or single-ended signals
  - Up to eight 4X gigabit serial ports
- One XMC mezzanine site

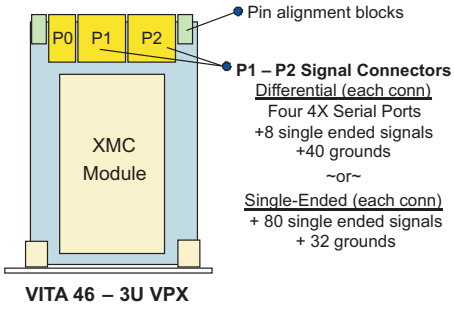

Figure 5

6U VPX Board

- 6U board outline same as 6U VME
- P0 Utility Connector
  - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT2 for P1 through P6 Signal Connectors
  - Definitions for differential or single-ended signals
  - Up to 24 4X gigabit serial ports
- One or two XMC mezzanine sites

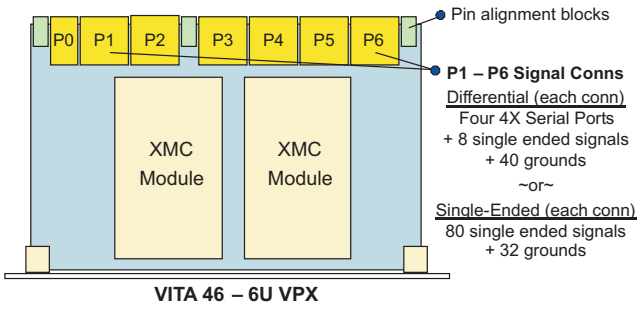

Figure 6

The 3U board outline is the same as the 3U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 3U board has two MultiGig RT2 Signal connectors, P1 and P2. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of eight 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 3U VPX board has one XMC mezzanine site that accepts one XMC module.

The 6U board outline is the same as the 6U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 6U board has six Multi-Gig RT2 Signal connectors P1 through P6. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of 24 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 6U VPX board has two XMC mezzanine site and accepts one or two XMC modules.

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OpenVPX Pipes

- Pipes
  - A grouping of differential pairs for an interconnect channel
  - Does not specify fabric protocols

Pipe Name	Abbreviation	# Diff Pairs	Also used
Ultra Thin Pipe	UTP	1	X1
Thin Pipe	TP	2	X2
Fat Pipe	FP	4	X4
Double Fat Pipe	DFP	8	X8
Quad Fat Pipe	QFP	16	X16
Octal Fat Pipe	OFP	32	X32

Figure 7

OpenVPX Connector Layout

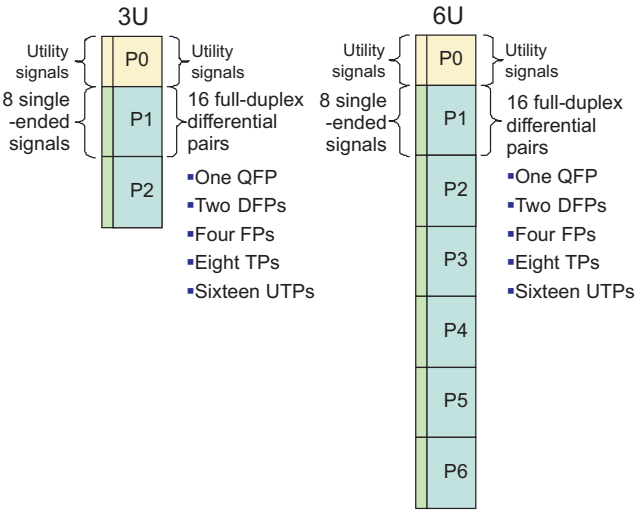


Figure 8

The OpenVPX Pipes are groups of differential pairs that are used to interconnect channels. As shown in the figure above, the defined OpenVPX pipe sizes range from one lane (1X) called an “ultra-thin pipe” or UTP, up to 32 lanes (32X) called an “octal fat pipe” or OFP.

The next size up from UTP is the “thin pipe” or TP which has two lanes or 2X. The popular 4X link is called a “fat pipe” or FP. The next size up from it is the “double fat pipe” or DFP with 8X links.

Next in size is the “quad fat pipe”, QFP or 16X and the fattest one is the “octal fat pipe”, OFP or 32X.

As used here and elsewhere in this handbook, the designation NX is the same as XN, or xN, where N is the number of lanes/pipes; The last designation, xN, is most commonly used with PCI Express.

Shown here are the connector layouts for the 3U and 6U cards.

As shown previously, the 3U card has one utility connector for utilities such as power, clock, etc. It also has two signal connectors P1 and P2. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

Likewise, the 6U board has the same utility connector and six signal connectors P1 through P6. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

Typical OpenVPX Backplane Profile

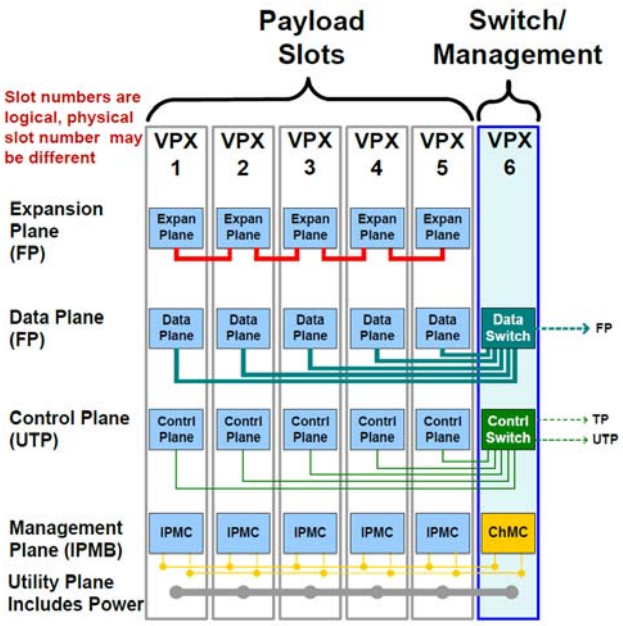


Figure 9

Typical OpenVPX Module Profile

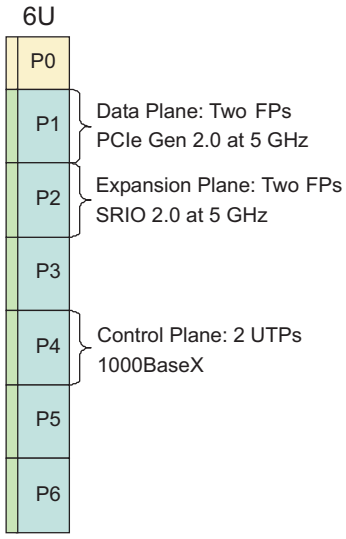


Figure 10

The OpenVPX specification established quite a large number of backplane profiles. The backplane profile is a physical definition of a backplane implementation. Included in this definition are:

- Slot sizes such as 3U or 6U
- Slot spacing such as 1.00, 0.85, or 0.80 inches
- Quantity of slots and type of slots
- Topologies used to interconnect the slots, such as:
  - Mesh
  - Central switch
  - Distributed
  - Root-leaf

Shown here is a typical 6-slot backplane with five payload cards and one switch/management card. Backplanes such as this one are primarily intended for development environments. However, some systems could be deployed in the field with these backplanes.

In addition to the backplane profiles, OpenVPX specifies module profiles. The module profile provides a physical mapping of ports into the module's backplane connectors. The module profile includes the assignment of specific protocols used for each port. It also provides first-order compatibility checks between modules and slots.

The typical module profile above shows the assignments for P1, P2, and P4. P0 is used for the utility functions. The assignments for the balance of connectors may be user-specified to suit the application.

XMC: Switched Serial Fabric for PMC

VITA Doc	Description
42.0	Base Specification: connectors, mechanical, etc.
42.1	Parallel RapidIO Protocol Layer
42.2	Serial RapidIO Protocol Layer
42.3	PCI Express Protocol Layer
42.6	10 GbE Protocol Layer
42.10	General Purpose I/O

Figure 11

Defined under VITA 42.0, the XMC specification extends the PMC card by adding new connections to support gigabit serial interfaces plus a growing list of alternative I/O standards.

As shown in the figure above, VITA 42.0 is the base specification that includes general information, reference and inheritance documentation, dimensional specifications, connectors, pin numbering and primary allocation of pairing and grouping of pin functions.

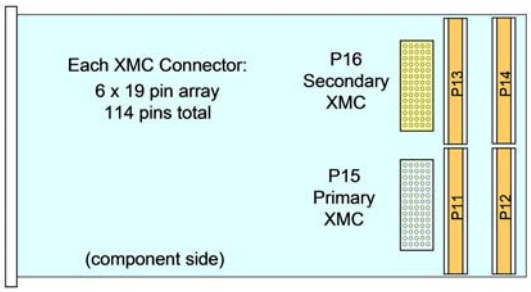
As of this writing VITA 42.0 and all subspecifications except 42.10 have been approved by VITA and ratified by ANSI. Subspecification 42.10 has been withdrawn.

XMCs can be single- or double-width modules that use a pin-socket connector with 114 pins arranged in a 6 x 19 array. A single-width XMC can have one or two connectors with pin functions as shown in Figure 12. A double-width XMC can have up to four connectors.

To support gigabit serial interfaces, notice that both P15 and P16 connectors define 10 full-duplex differential pair lines. The VITA 42.0 base specification does not dictate signal types, data rates, protocols, voltage levels or grouping for these signals. Instead, it wisely leaves that up to the several subspecifications that follow, allowing XMCs to evolve as new standards emerge.

In fact, contrary to the fundamental mission of supporting serial interfaces, the first subspecification, VITA 42.1, defines these same pins for Parallel RapidIO.

PMC/XMC Connector Definition



P15 Primary XMC Connector

- 10 differential pairs each direction
- JTAG
- System Management
- Auxiliary
- 3.3 V Power:
  - Main: 4 pins, 1 A/pin, 13.2 W
  - Auxiliary: 1 pin, for system management
- Variable Power
  - 8 pins, 1 A/pin
  - 5 V (40 W max) or 12 V (96 W max)
  - Modules must accept 5 V or 12 V
  - Carriers may provide 5 V or 12 V

P16: Secondary XMC Connector

- 10 more differential pairs each direction
- High-speed or single-ended user I/O
- Extensions of gigabit serial fabrics

Figure 12

While VITA 42.1 is approved and fielded, few vendors have embraced this standard and have instead opted for the more popular serial protocols.

As shown in Figure 12, most of the pins on P15 are reserved for serial links, power and other functions, but P16 has a wealth of user-defined pins now being addressed by the VITA 42.10 General Purpose I/O draft specification. It offers a standardized way of implementing interfaces for popular system I/O including Ethernet, USB ports, RS-232, RS-485, Serial ATA, Fibre Channel, and SAS (Serial Attached SCSI). The clear benefit here is that by following these definitions, XMC and carrier board designers can achieve a much wider range of interoperability, the essential goal of industry standards.

VPX Specification Status

▪ VITA 46.0 – VPX Baseline Specification	Approved
• VITA 46.1 VMEbus Signal Mapping	Approved
• VITA 46.3 4x Serial RapidIO Signal Mapping	Approved
• VITA 46.4 PCI Express Signal Mapping	Approved
• VITA 46.6 Gbit Ethernet Control Plane Signal Mapping	Approved
• VITA 46.7 10Gbit Ethernet Signal Mapping	Approved
• VITA 46.8 Infiniband	Draft
• VITA 46.9 PMC/XMC Rear I/O Fabric Signal Mapping	Approved
• VITA 46.10 Rear Transition Module	Approved
• VITA 46.11 System Management	Approved
▪ VITA 48.0 – REDI – Baseline Specification	Approved
• VITA 48.1 REDI Air Cooling	Approved
• VITA 48.2 REDI Conduction Cooling	Approved
• VITA 48.3 REDI Liquid Cooling	Draft
• VITA 48.4 REDI Mech Spec for Liquid Flow Through	Draft
• VITA 48.5 Air Flow Through Cooling	Approved
• VITA 48.7 Air Flow-By Cooling	Approved
• VITA 48.8 Mechanical Spec Using Air Flow-By Cooling	Approved
▪ VITA 49.0 – VITA Radio Transport (VRT)	Approved
• VITA 49.1 VITA Radio Link (VRL)	Approved
• VITA 49.2 VITA Radio Transport Control Packets	Draft
▪ VITA 60.0 – VPX: Alterative Connector for VPX	Approved
▪ VITA 62.0 – VPX: Power supply	Approved
▪ VITA 63.0 – VPX: KVPX, Alternate Connector for VPX	Approved
▪ VITA 65.0 – OpenVPX	Approved
• VITA 65.0 - Base Specification	Approved
▪ VITA 66.0 – Optical Interconnect on VPX	Approved
• VITA 66.0 Optical Interconnect on VPX, Base Spec	Approved
• VITA 66.1 Optical Interconnect on VPX, MT Variant	Approved
• VITA 66.2 Optical Interconnect on VPX, Airinc Variant	Approved
• VITA 66.3 Optical Interconnect on VPX, Beam Variant	Approved
• VITA 66.4 Optical Interconnect on VPX, Half Width Bm Var	Approved
▪ VITA 67.0 – Coaxial Interconnect on VPX	Approved
• VITA 67.0 Coaxial Interconnect on VPX, Base Spec	Approved
• VITA 67.1 Coaxial Interconnect on VPX, 3U	Approved
• VITA 67.2 Coaxial Interconnect on VPX, 6U 8 Position	Approved
• VITA 67.3 Coaxial Interconnect on VPX, 6U 4 Position	Draft
▪ VITA 68.0 – VPX: Compliance Channel	Draft

Figure 13

As of this writing, the VPX Baseline Specification has been approved by VITA, ratified by ANSI and has been released as VITA 46.0. Most of its subspecifications have also been approved.

Likewise, the VITA 48.0 REDI is approved. Also approved are most of its subspecifications.

Also, the OpenVPX VITA 65.0 Base Specification has been approved by VITA and ratified by ANSI.

Two more VITA standards have been approved: VITA 66.0 Optical Interconnect on VPX and VITA 67.0 Coaxial Interconnect on VPX. The latter was initiated by DRS. Pentek has been actively involved in the development of this specification.

For the latest and most up-to-date specifications regarding VITA/ANSI standards, contact:
VITA

http://www.vita.com/Standards

VPX, VPX REDI, OpenVPX

1. Why was OpenVPX created in the first place?

The US Department of Defense and other users are mandating improved implementation of open standards and interoperability. VPX specifications have been focused at the board level, but there is also a need for considering system-level requirements to improve interoperability and reduce customization, testing, cost, and risk.

2. What are the general OpenVPX features?

- OpenVPX is a defined set of system implementations within VPX
- Specifies a set of system architectures
- Uses existing VPX REDI standards and drafts with minimal possible changes
- Defines multiple planes for Utility, Management, Control, Data, Expansion
- Defines various sizes of pipes used for serial communication
- Defines several types of profiles for structure and hierarchy in the specification (slot profile, backplane profile, module profile, development chassis profile)
- Backplane profiles define the backplane topology (types: centralized and distributed switching, and host/slave)

3. Does OpenVPX replace VPX?

No. OpenVPX is a system specification for VPX that provides a defined framework for interoperability between OpenVPX products. OpenVPX leverages the VPX dot specs for details such as fabric protocols.

4. What's the difference between VPX and OpenVPX?

OpenVPX builds on VPX dot specs and provides a defined framework for interoperability between OpenVPX products based on compatible OpenVPX profiles for modules, backplanes, and development chassis.

5. What is an OpenVPX module profile?

An OpenVPX module profile is a physical mapping of Ports onto a given Module's backplane Connectors and protocol mapping(s), as appropriate, to the assigned Port(s). This definition provides a first-order check of operating compatibility between modules and slots as well as between multiple modules in a chassis. Profile parameters are used to further describe properties of a Module Profile.

6. What is an OpenVPX backplane profile?

An OpenVPX backplane profile is a physical definition of a backplane implementation that includes details such as the number and type of slots that are implemented and the topologies used to interconnect them. Ultimately a Backplane Profile is a description of channels and buses that interconnect slots and other physical entities in a backplane. Profile parameters are used to further describe properties of a backplane profile.

7. What are OpenVPX pipes used for?

OpenVPX pipes are a physical aggregation of differential pairs used for common function that is characterized in terms of the total number of differential pairs. A pipe is not characterized by the protocol used on it. The following pipes are predefined by OpenVPX: Ultra Thin Pipe (UTP), Thin Pipe (TP), Fat Pipe (FP), Double Fat Pipe (DFP), Quad Fat Pipe (QFP), Octal Fat Pipe (OFP).

8. What styles of OpenVPX backplanes are available?

OpenVPX backplanes are available in lengths between one and twenty-one slots. On most standard backplanes, boards are located on 1.0" centers (i.e. 1.0" pitch), though 0.8" pitch or 0.85" pitch may also be used. Backplanes are available in 3U and 6U form factors. Furthermore, there are many different profiles available for OpenVPX backplanes:

- Central switch topologies
- Distributed topologies
- Root-leaf topologies

9. Can I get conduction-cooled OpenVPX hardware?

Yes. A popular OpenVPX card style is the conduction-cooled module. These are used mainly in military and aerospace applications where convection cooling cannot be used. These allow heat to conduct through the printed circuit board or through a conduction plate on the module. Expanding wedge locks then transfer the heat out to the chassis through wide slots cut into the metal chassis sidewalls.

10. What are the OpenVPX connector pin assignments?

OpenVPX connector pin assignments are defined in several slot profiles aimed at different types of slots:

- Payload slot profiles
- Switch slot profiles
- Peripheral slot profiles

11. What power supplies are available on the backplane?

The same as VPX with the exception that OpenVPX currently does not support the 48V power option for 6U modules. OpenVPX also encourages more standardization in the use of the primary power rails but the rails are unchanged from VPX.

(These Frequently Asked Questions Courtesy of VITA)

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Optical Resources

Optical Links Offer Many Benefits

Property	Copper	Optical
Interface Transceiver Cost	Low ✓	High but dropping
PC Network Interface Cards	Integrated in PC or laptop ✓	Usually optional at $100-$200
Power over Ethernet	Supported at low cost ✓	Not possible
Data Rate	1 GHz	>10 GHz ✓
Cable Loss - 100 meters	94%	3% ✓
Max Transmission Distance	100 m (cat 6)	300 m (multi-mode) 10 km (single mode) ✓
EMI Susceptibility Risk	Moderate	Zero ✓
EMI Radiation Risk	Moderate	Zero ✓
Security / Eavesdropping Risk	High	Extremely Low ✓
Termination Costs	Low ✓	High
Cable Cost per Length	High	Low ✓
Cable Weight per 1000 m	60 to 600 kg	6 kg ✓
Fire Hazard	Supports current flow if shorted	Zero ✓
Tensile Strength	25 pounds	100-250 pounds ✓
Cleaning Requirements	No ✓	Yes

Figure 14

One major shortcoming of copper cable is signal loss, which becomes a serious limitation for higher frequency signals and longer cable lengths. Across a span of 100 meters, optical cables can sustain data rates up to 100 times higher than copper cable.

Because copper cables radiate electromagnetic energy, eavesdropping on network cables is a major security concern, not only for military and government customers, but also for corporations, banks, and financial institutions. Advanced signal sniffers in vehicles and briefcases are hard to detect and restrict. Optical cables are extremely difficult to "tap" without damaging the cable, resulting in immediate detection.

Signals flowing in copper cables are also susceptible to contamination from nearby sources of electromagnetic radiation, such as antennas, generators, and motors. This is critical for military and commercial aircraft and ships, as well as manned or unmanned vehicles, which are often packed with dozens of different electronic payloads. Optical cables are completely immune to EMI.

Physically, optical cables are much smaller and lighter than copper cables, especially important for weight-sensitive applications such as weapons, unmanned vehicles, and aircraft. Optical cables will operate just as well when submerged in seawater, and are completely immune to electrical shorting, especially important where explosive vapors may be present. To ease installation through conduits and passages, optical cables have smaller diameters and can withstand up to ten times more pulling tension than copper cables.

Driven by huge commercial markets for data servers, storage networks, telecom systems, and home or office internet and entertainment systems, optical interfaces are replacing older copper connections for good reasons: cost and performance. As the use of optical cables becomes more widespread, the cost per length can be much lower than copper cables that depend on commodity metal pricing. As is often the case, industrial, military and government embedded systems are now taking advantage of the many benefits of this rapidly advancing commercial technology.

Optical Resources

Optical Cables

Figure 15

The Pentek Model 52611 Quad SerialFPDP 3U VPX module supports four full-duplex LC optical cables for connections between chassis, each operating at over 400 MB/sec

An optical cable is a waveguide for propagating light through an optical fibre. It consists of a central core clad with a dielectric material having a higher index of refraction than the core to ensure total internal reflection. Optical cables use either multi-mode or single-mode transmission.

Multi-mode cables accept light rays entering the core within a certain angle of the axis. They travel down the cable by repeatedly reflecting off the dielectric boundary between the core and the cladding. The core diameters are typically 50 or 62.5 mm, and the wavelength of light is typically 850 nm.

Single-mode cables propagate light as an electromagnetic wave operating in a single transverse mode straight down the fibre using typical wavelengths of 1310 and 1550 nm. The core diameter must be no greater than ten times the light wavelength, typically 8 to 10 µm. Although single-mode cables can carry signals over lengths 10 to 100 times longer than multi-mode, the transceivers are more expensive.

Hundreds of different types of optical cable connectors exist in the market, each addressing specific applications and environments. The challenge is connecting the ends of two optical cables to retain the maximum fidelity of the light interface, in spite of human factors, tolerances, contamination, and environments. Special tools and kits for cleaning the ends of each optical fibre are essential for reliable operation.

Optical Transceivers

Coupling electrical signals to light signals for transmission through optical cables requires optical transceivers. Most systems require full-duplex operation for each optical link to support flow-control and error correction. A pair of optical fibers, often bonded together in the same cable, supports transmit and receive data flowing in opposite directions.

Although several analog light modulation schemes (including AM and FM) have been used in the past, now almost all transceivers use digital modulation. Optical emitters simply translate the digital logic levels into on/off modulation of the laser light beam, while the detectors convert the modulated light back into digital signals. This physical layer interface for transporting 0s and1s is capable of supporting any protocol.

The latest transceivers use laser emitters to support data rates to 100 Gbits/sec and higher, and each generation steadily reduces the power, size and cost of devices. Different technologies are required for emitters and detectors, but both are often combined in a single product to provide full-duplex operation.

Optical transceivers thus provide a physical layer interface between optical cables and the vast array of electrical multi-gigabit serial ports found on processors, FPGAs, and network adapters. As a result, optical transceivers are transparent to the protocols they support, making them appropriate for any high-speed serial digital link.

Electrical signals of the optical transceivers connect to the end point device, which must then handle clock encoding and recovery, synchronization, and line balance at the physical layer. Data link layer circuitry establishes framing so that data words can be sent and received across the channel.

Choosing the Right Optical Protocol

Protocols define the rules and features supported by each type of system link, ranging from simple transmission of raw data to sophisticated multi-processor support for distributed networks, intelligent routing, and robust error correction. Of course, heavier protocols invariably mean less efficient data transfers and increased latency. Generally, it is best to use the simplest protocol that satisfies the system requirements.

As an example of a lightweight protocol, Aurora for Xilinx FPGAs features on-board link-layer engines and high-speed serial transceivers. Aurora is intended primarily for point-to-point connectivity for sending data between two FPGAs. It includes 8b/10b or 64b/66b channel coding to balance the transmission channel, and supports single- or full-duplex operation. Aurora handles virtually any word length and allows multiple serial lanes to be bonded into a single logical channel, aggregating single lane bit rates for higher data throughput. Data rates for each serial lane can be 12.5 Gbits/sec or higher. Extremely simple and with minimal overhead, Aurora is very efficient in linking data streams between multiple FPGAs within a module, or between modules across a backplane.

Stepping up in complexity is the SerialFPDP protocol defined under VITA 17.1 It addresses several important needs of embedded systems including flow control to avoid data overruns, and copy mode to allow one node to receive data and also forward it on to another node. The copy/loop mode supports a ring of multiple nodes eventually completing a closed loop. The nominal data rate on each lane is 2.5 Gbits/sec, but advances in device technology now support rates over twice that speed.

Infiniband defines a flexible, low-latency, point-to-point interconnect fabric for data storage and servers with current rates of 14 Gbits/sec, moving up to 50 Gbits/sec in the next few years. Channel speeds can be boosted by forming logical channels by bonding 4 or 12 lanes.

The venerable Ethernet protocol still dominates computer networks, with 10GbE now commonly supported by a vast range of computers, switches, and adapters. Even though Ethernet suffers from high overhead, making it somewhat cumbersome for high-data rate low-latency applications, its ubiquitous presence virtually assures compatibility.

VITA 49.0: VITA Radio Transport (VRT) Standard

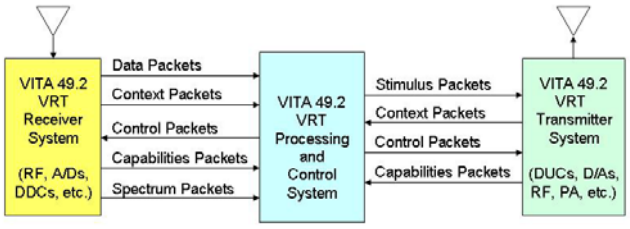


Figure 16

New extensions to the VITA VRT Protocol define standardized packets for control and status of radio receiver and transmitter equipment and digitized receive and transmit signal payload packets for added flexibility

Approved as an ANSI standard in 2007, VITA 49.0 defines standardized packets for connecting software radio systems for communications, radar, telemetry, direction finding, and other applications. The original specification addressed only receiver functions. Receive signal data packets deliver digitized payload data, a precise time stamp, and identifiers for each channel and signal. Context packets include operating parameters of the receiver including tuning frequency, bandwidth, sampling rate, gain, antenna orientation, speed, heading, etc. One notable shortcoming of the original specification was its inability to control the receiver.

VITA 49.2, a new extension to VRT now in balloting, adds control packets for delivering operational parameters to all aspects of the radio equipment, as well as support for transmitters. The new stimulus packets contain streaming digital samples of signals to be transmitted. Other new packets, called capabilities packets, inform the host control system of the available hardware in the radio along with the allowed range of parameters for control. Lastly, spectrum packets from the receiver deliver spectral information to help simplify spectral survey and energy detection operations required by the control system.

With this latest extension, VRT provides a standardized protocol for controlling and configuring all aspects of a software-radio transceiver. One major objective is enabling a common radio hardware platform to handle a wide range of applications simply by implementing new host software algorithms that exploit VRT protocols to achieve the required modes of operation.

Optical Resources

Optical Interfaces for VPX

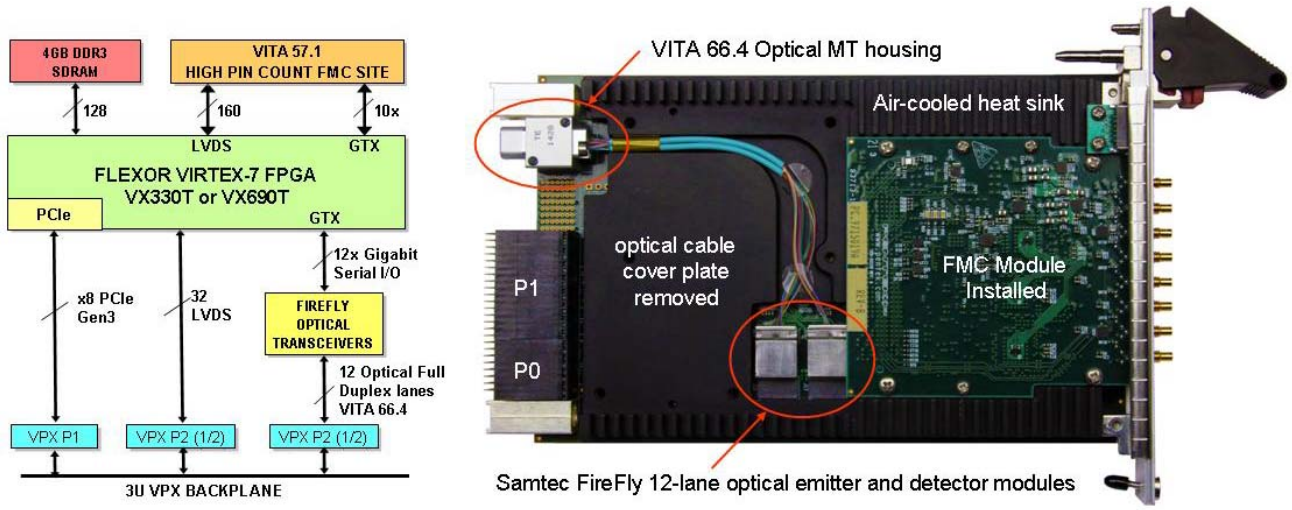


Figure 17

Although optical interfaces using various connectors and cable types have been deployed in embedded systems for years, most of them use front panel connections. This can be a maintenance issue and is often not permitted in conduction-cooled systems.

The VITA 66 Fiber Optic Interconnect group has developed a set of standards that bridge optical connections directly through the VPX backplane connector. The first three are variants for 3U and 6U systems and are based on MT, ARINC 801 Termini, and Mini-Expanded Beam optical connector technology, respectively.

The metal housings are physically dimensioned to replace one or more of the standard MultiGig RT-2 VPX bladed copper connectors. The high-density MT variant defined in VITA 66.1 provides the highest density of the three, with up to 12 or 24 pairs of optical fibers, while VITA 66.2 and 66.3 each provide 2 pairs.

A fourth standard soon to be released, VITA 66.4, uses the MT ferrule but with a metal housing half the size of VITA 66.1, thus occupying only half of the 3U VPX P2 connector position.

To simplify implementation, Samtec offers its FireFly™ Micro Fly-Over system. It consists of 12 pairs of optical fibers installed in an MT ferrule. One 12-lane optical flat cable connects to a small VCSEL laser emitter module and the other connects to a detector module.

Figure 17 shows the industry's first implementation of the emerging VITA 66.4 standard, the Pentek Model 5973 3U VPX Virtex-7 FMC carrier. Here the electrical interfaces of the FireFly emitter and detector modules are connected directly to the GTX serial transceiver pins of the Virtex-7 FPGA. Today, FireFly transceivers are rated for 14 Gbits/sec with 28 Gbits/sec versions coming soon. With the 5973 operating at nominal data rates of 10 Gbits/sec through each optical fibre using Aurora protocol, the backplane throughput is 12 GB/sec, simultaneously in both directions.

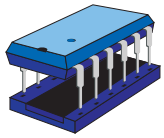
The first version of this product uses multi-mode transceivers and cable to support cable lengths of 100 meters or more. Single-mode transceivers will extend the distance to several kilometers. A wide range of MT optical cables and connector products allow board-to-board connections across the backplane, and backplane-to-chassis connections for external MTP cables to remotely located systems.

The 12 GB/sec VITA 66.4 optical interface complements the 8 GB/sec Gen 3 x8 copper PCIe interface on VPX P1, offering plenty of I/O for demanding applications. System engineers can now choose between optical and copper links to solve high-data rate connectivity requirements.

FPGA Resources

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
  - Control logic
  - Glue logic
  - Registers and gates
  - State machines
  - Counters and dividers



- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

Figure 18

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
  - Schematic processors
  - Boolean processors
  - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
  - Critical paths and propagation delays
  - Pin assignment and pin locking
  - Signal loading and drive capabilities
  - Clock distribution
  - Input signal synchronization and skew analysis

Figure 19

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

FPGA Resources

FPGAs: New Device Technology

- 500+ MHz DSP slices and memory structures
- Over 3500 dedicated on-chip hardware multipliers
- On-board GHz serial transceivers
- Partial reconfigurability maintains operation during changes
- Switched fabric interface engines
- Over 690,000 logic cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC microcontroller cores
- Memory densities approaching 85 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 28 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards

Figure 20

FPGAs: New Development Tools

- High Level Design Tools
  - Block Diagram System Generators
  - Schematic Processors
  - High-level language compilers for VHDL & Verilog
  - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - Faster compilers and simulators save time
  - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
  - FPGA vendors offer both free and licensed cores
  - FPGA vendors promote third party core vendors
  - Wide range of IP cores available

Figure 21

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you'll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking below 0.1 micron.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

FPGA Resources

FPGA Resource Comparison

	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX	Kintex KU035, 60,115
Logic Cells	52K–155K	128K–314K	326K–693K	444K–1,451K
CLB Flip-Flops	32K–96K	160K–392K	408K–864K	406K –1,326K
Slices*	8K–24K	20K–49K	51K–108K	69K–207K
Block RAM (kb)	4,752–8,784	9,504–25,344	27,000–52,920	19,000–75,900
DSP Slices	128–640	480–1,344	1,120–3,600	1,700–5,520
Serial Gbit Transceivers	12–16	20–24	28–80	16–64
PCI Express Support	N/A	Gen 2 x8	Gen 2 x8, Gen3 x8	Gen 2 x8, Gen3 x8
Max. User I/O	480–680	600–720	700–1,000	416–676

*Virtex-5, Virtex-6, Virtex-7 and Kintex Slices actually represent 6.4 Logic Cells

Figure 22

The above chart compares the available resources in the four Xilinx FPGA families that are used or have been used in most of Pentek products.

- Virtex-5: LX and SX
- Virtex-6: LX and SX
- Virtex-7: VX
- Kintex UltraScale: KU035, KU060, KU115

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 550 MHz in V-5 to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.

The Kintex UltraScale devices offer even more performance than the Virtex-6 and Virtex-7 with less power dissipation.

The Kintex series offer PCIe Gen 2 and Gen 3 and provide a peak speed of 8 GB/sec. Pentek offers the KU035 as standard with the Kintex-based Jade products, while the KU060 and KU115 are offered as optional. The KU115 offers 5,520 DSP slices that should be enough to satisfy just about any signal-processing requirement.

FPGA Resources

GateFlow FPGA Design Resources

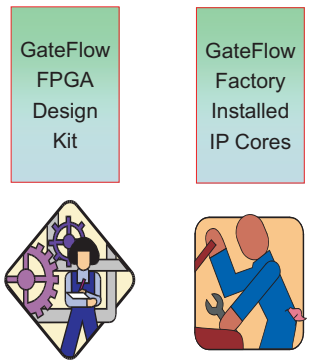


Figure 23

GateFlow FPGA Design Kit

- Allows FPGA design engineers to easily add functions to standard factory configuration
- Includes VHDL source code for all standard functions:
  - Control and status registers
  - A/D and Digital receiver interfaces
  - Mezzanine interfaces
  - Triggering, clocking, sync and gating functions
  - Data packing and formatting
  - Channel selection
  - A/D / Receiver multiplexing
  - Interrupt generation
  - Data tagging and channel ID
- **User Block** for inserting custom code

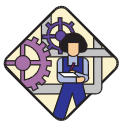


Figure 24

GateFlow® is Pentek's flagship collection of FPGA Design Resources. The GateFlow line is compatible with the Xilinx Virtex products and is available as two separate offerings:

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

We also offer popular high-performance signal-processing algorithms with the GateFlow factory-installed IP Cores. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products

Installed Cores are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully supported with Pentek ReadyFlow® Board Support Packages.

Let's start with the GateFlow FPGA Design Kit.

GateFlow
ReadyFlow Board Support Package

If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, and data tagging.

These are also fully supported with our ReadyFlow Board Support Package.

We also include a special User Block, positioned right in the data stream, so you can easily drop in your own custom signal processing algorithms.

FPGA Resources

GateFlow FPGA Design Kit for Cobalt, Onyx, Jade and Flexor Products

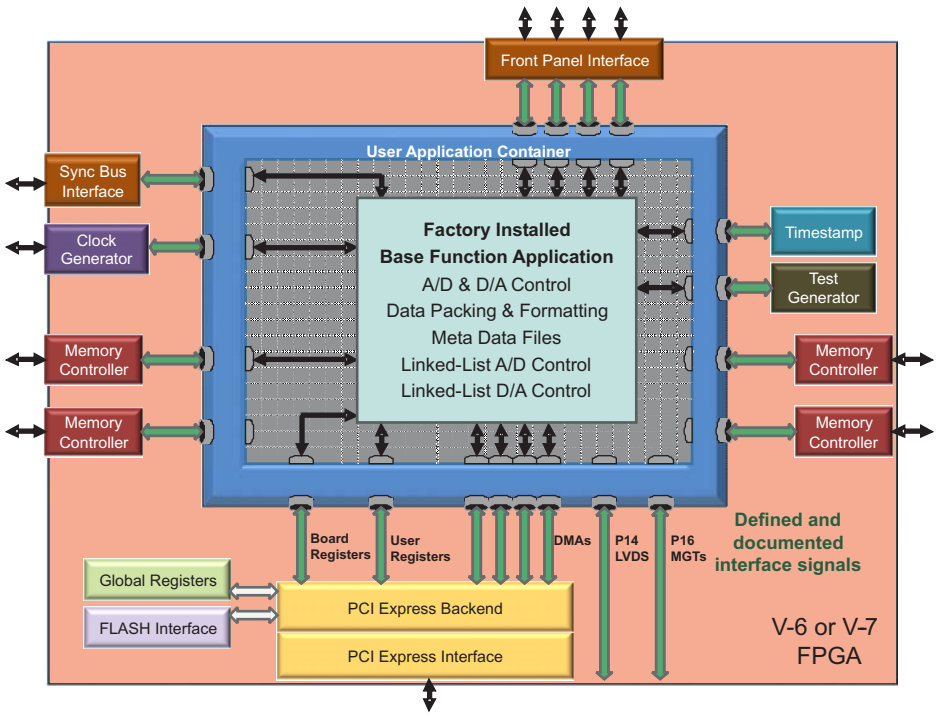


Figure 25

The **GateFlow** FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt, Onyx, Jade and Flexor architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

Shown here is the FPGA block diagram of a typical Cobalt, Onyx, Jade or Flexor module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each module provides an example of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.

FPGA Resources

GateFlow Installed IP Cores

- Pentek Installs IP Cores in Pentek Products
- Cores are tailored and optimized for:
  - Specific devices and I/O found on Pentek products
  - Efficient FPGA resource utilization
  - Execution and throughput speed
- Eliminates need for customer FPGA development
- Fully supported with ReadyFlow Board Support Libraries

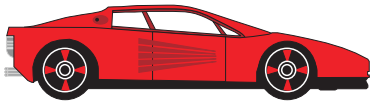


Figure 26

Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

Pentek offers popular high-performance signal processing algorithms installed in Pentek products. These algorithms are designed expressly for Xilinx FPGAs and Pentek harware products. The cores take full advantage of the numerous hardware multipliers to achieve highly-parallel processing structures that can dramatically outperform programmable RISC and DSP processors.

Installed Cores are optimized for efficient FPGA resource utilization, execution and throughput speed. They are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully tested and supported with the Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.

VPX, PMC/XMC, PCI Express, AMC, FMC, and CompactPCI Software Radio and Supporting Products

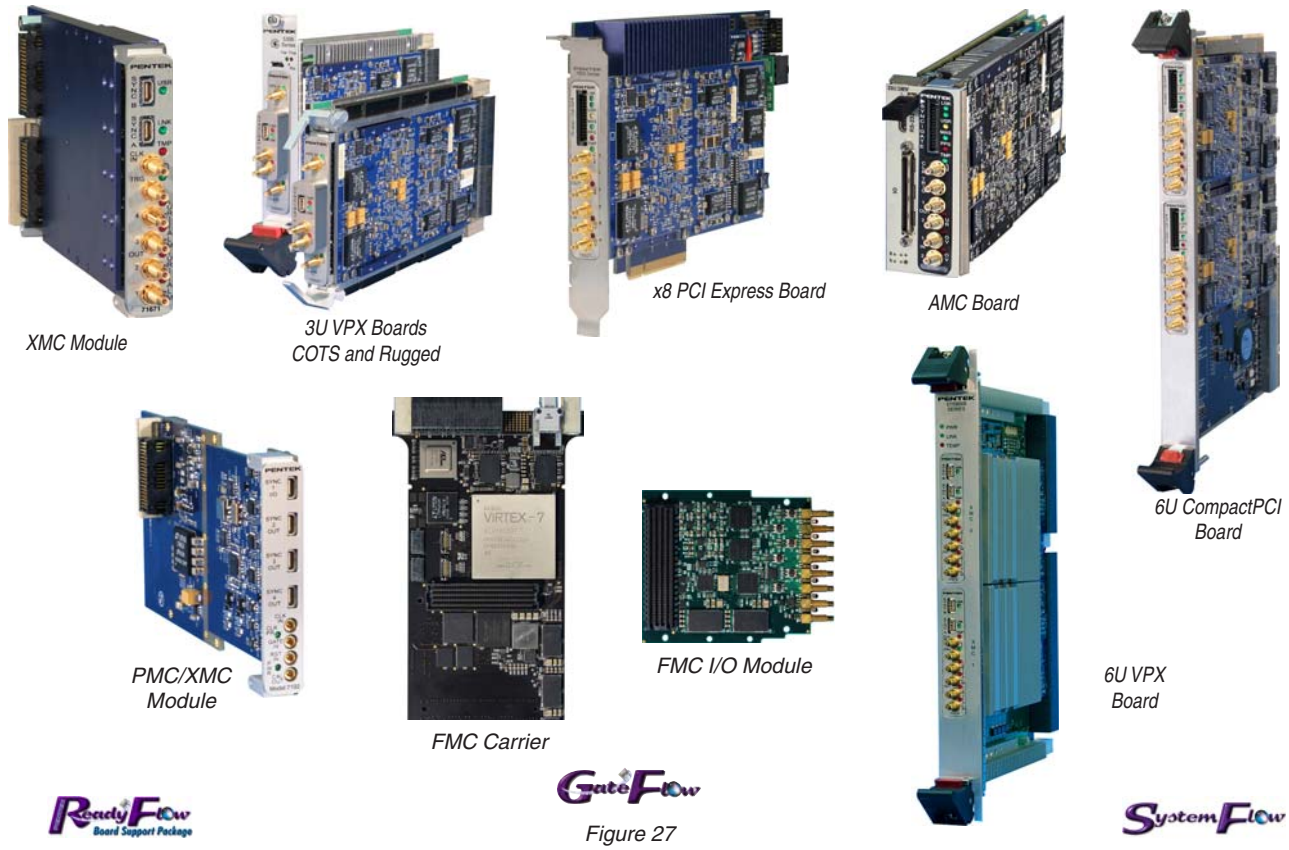


Figure 27

The Pentek family of board-level software radio products is the most comprehensive in the industry. All of these products are available in several formats to satisfy a wide range of requirements: 3U and 6U VPX, PMC/XMC, PCI Express, AMC, FMC, 3U and 6U CompactPCI.

Software radio products are supported by clock synthesizer, synchronizer and distribution boards. These products are also available in the same formats as the software radio products.

In addition to their commercial versions, many of the above products are available in ruggedized versions up to and including conduction-cooled.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow® Board Support Package, the GateFlow® FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek high-speed recording systems are supported with SystemFlow® recording software that features a Windows®-based graphical user interface.

In addition to the product overviews presented in the pages that follow, active links to their datasheets and the datasheets of similar products on Pentek's website, are included with each product.

Cobalt, Onyx and Jade XMC Models

Model	Cobalt	Onyx	Jade	A/D Converters #	A/D Converters Type	D/A Converters #	D/A Converters Type	IP or Other I/O Type
71x20	✓	✓	✗	3	200 MHz / 16-bit	2	800 MHz / 16-bit	
71x21	✓	✓	✓	3	200 MHz / 16-bit	2	800 MHz / 16-bit	DDC, Interp, Sum
71x24	✓	✗	✗	3	200 MHz / 16-bit	2	800 MHz / 16-bit	Adaptive Relay
71x60	✓	✓	✗	4	200 MHz / 16-bit			
71x61	✓	✓	✓	4	200 MHz / 16-bit			DDC, Sum
71x62	✓			4	200 MHz / 16-bit			DDC
71x63	✓	✗	✗	4	200 MHz / 16-bit			GSM Channelizer
71x64	✓			4	200 MHz / 16-bit			DDC, VITA-49
71x90	✓			2	200 MHz / 16-bit			.925 – 2.175 GHz L-Band Tuner
71x50-014	✓	✗	✗	2	400 MHz / 14-bit	2	800 MHz / 16-bit	
71x50	✓	✗	✗	2	500 MHz / 12-bit	2	800 MHz / 16-bit	
71x51-014	✓	✓	✓	2	400 MHz / 14-bit	2	800 MHz / 16-bit	DDC, Interp, Sum
71x51	✓	✓	✓	2	500 MHz / 12-bit	2	800 MHz / 16-bit	DDC, Interp, Sum
71x30	✓	✓	✓	1	1 GHz / 12-bit	1	1 GHz / 16-bit	
71x40	✓	✗	✗	1 2	3.6 GHz / 12-bit 1.8 GHz / 12-bit			
71x41	✓	✓	✓	1 2	3.6 GHz / 12-bit 1.8 GHz / 12-bit			DDC
71x70	✓	✗	✗			4	1.25 GHz / 16-bit	
71x71	✓	✓	✓			4	1.25 GHz / 16-bit	Interp
71x10	✓							32 pair LVDS I/O
71x11	✓							Quad Serial FPDP

Notes

- The chart above lists only the 71xxx XMC products that form the basis of all Cobalt, Onyx and Jade product lines.
- By changing the 2nd digit of the model number to "2", the 72xxx 6U cPCI products offer the same resources as the table above, plus an extra available XMC site.
- By changing the 2nd digit to "3", the 73xxx 3U cPCI products offer the same resources as the table above.
- By changing the second digit to "4" the 74xxx 6U cPCI products offer twice the resources shown in the table.
- By changing the 2nd digit to "8" the 78xxx PCIe products offer the same resources as the products in the table.
- By changing the 1st and 2nd digits to "52", the 52xxx 3U VPX products offer the same resources as the table.
- By changing the 1st and 2nd digits to "53", the 53xxx 3U VPX products offer a crossbar switch to the backplane.
- By changing the 1st and 2nd digits to "56", the 56xxx AMC products offer the same resources as shown in the table.
- By changing the 1st and 2nd digits to "57", the 57xxx 6U VPX products offer the same resources, plus an extra available XMC site.
- By changing the 1st and 2nd digits of the model number to "58", the 58xxx 6U VPX products offer twice the resources shown in the table above.

Figure 28

VPX Families for Cobalt Products

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Figure 29-A

Pentek offers two families of Cobalt® 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Cobalt products utilize the Xilinx Virtex-6 FPGA.

VPX Families for Onyx Products

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Figure 29-B

Pentek offers two families of Onyx® 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Onyx products utilize the Xilinx Virtex-7 FPGA.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

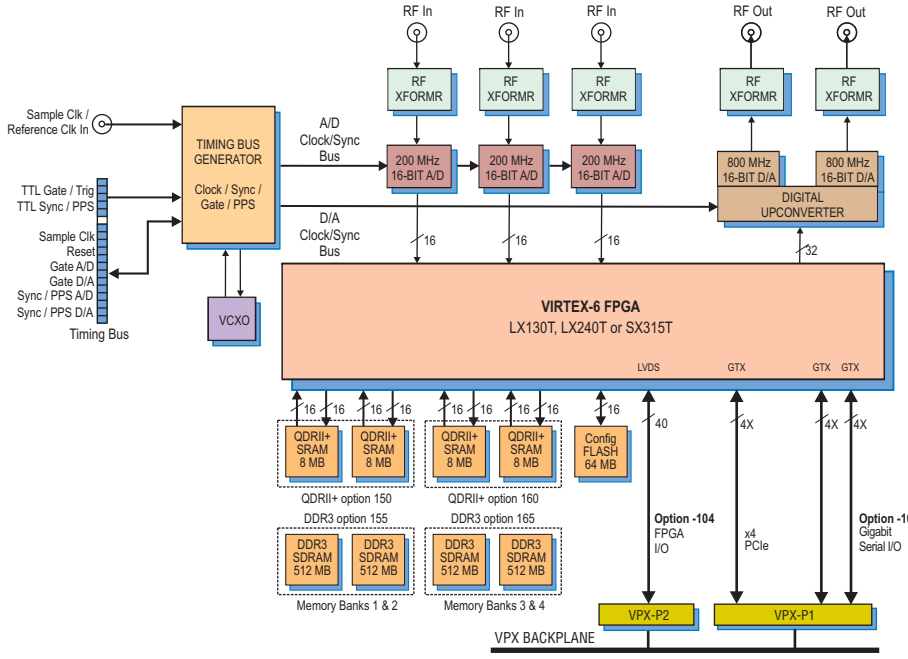
Figure 29-C

VPX Families for Jade Products

Pentek offers two families of Jade™ 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Jade products utilize the Xilinx Kintex UltraScale FPGA.

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 52620 - 3U VPX



Model 52620 3U VPX COTS and rugged

Figure 30

Model 52620 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 52620 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

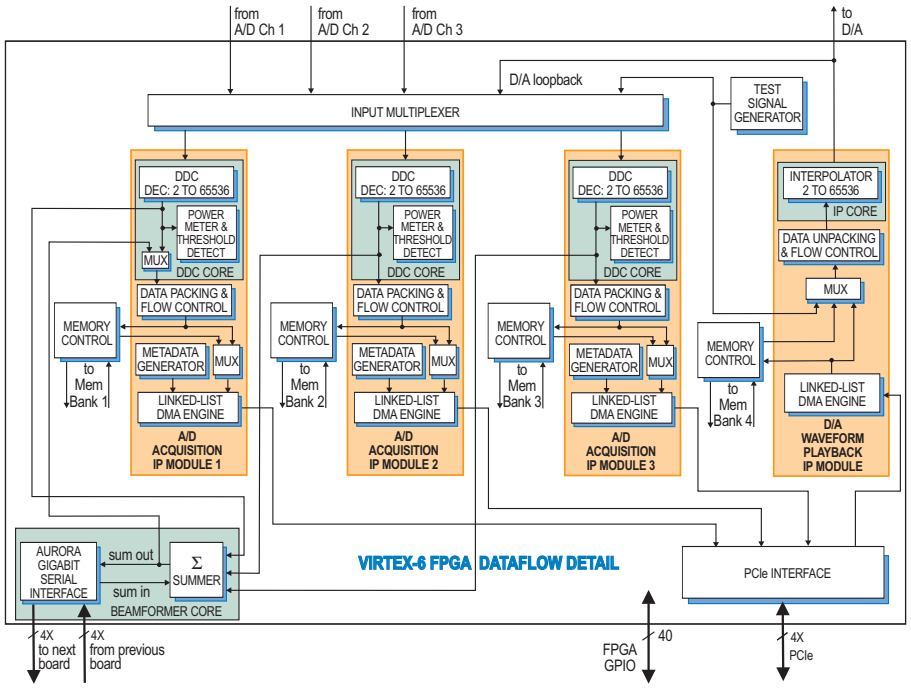
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 52620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or combinations.

Versions of the 52620 are available as another 3U VPX (Model 53620), 6U VPX (Models 57620 and 58620 dual density), XMC module (Model 71620), x8 PCIe (Model 78620), AMC (Model 56620), 6U cPCI (Models 72620 and 74620 dual density), and 3U cPCI (Model 73620).

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-6 FPGA

Model 52621 - 3U VPX



Model 52621 3U VPX
COTS and rugged

Figure 31

Model 52621 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 52620 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 52620 and address the requirements of many applications.

The 52621 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

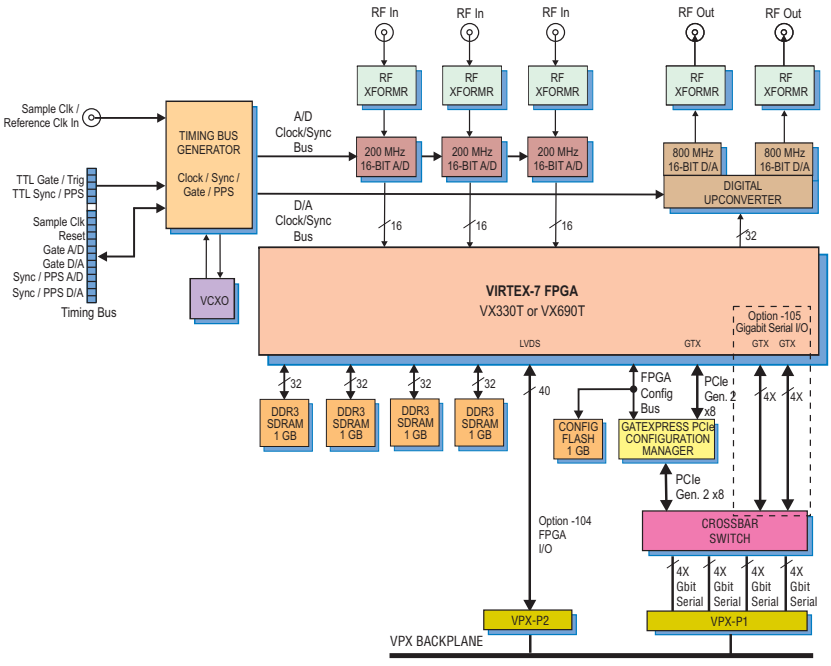
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 52621 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 52621 are available as another 3U VPX (Model 53621), 6U VPX (Models 57621 and 58621 dual density), XMC module (Model 71620), x8 PCIe (Model 78621), AMC (Model 56621), 6U cPCI (Models 72621 and 74621 dual density), and 3U cPCI (Model 73621).

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 53720 - 3U VPX



Model 53720 3U VPX COTS and rugged

See page 29

Figure 32

Model 53720 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

Multiple 53720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync.

Versions of the 53720 are also available as another 3U VPX (Model 52720), 6U VPX (Models 57720 and 58720 dual density), XMC (Model 71720), x8 PCIe board (Model 78720), AMC (Model 56720), 6U cPCI (Models 72720 and 74720 dual density), and 3U cPCI (Model 73620).

GateXpress® is a configuration manager for loading and reloading the Virtex-7 FPGA. More on page 30.

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-7 FPGA

Model 53721 - 3U VPX

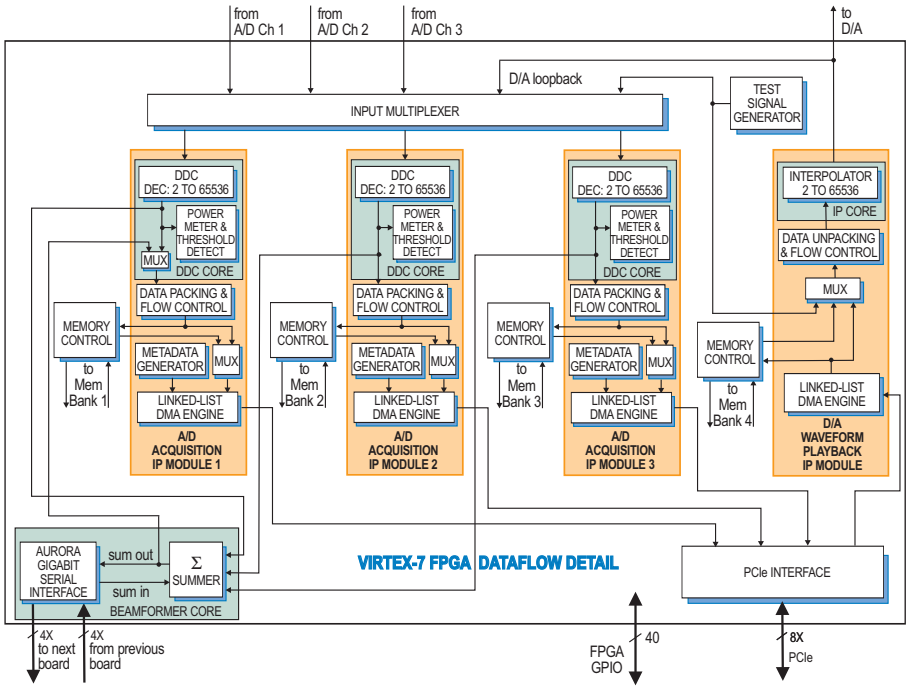


Figure 33

Model 53721 3U VPX
COTS and rugged

Onyx
GateXpress

See page 29

Model 53721 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter based on the Model 53720 described previously, it includes factory-installed IP cores to enhance the performance of the 53720 and address the requirements of many applications.

The 53721 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 53721 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 53721 are available as another 3U VPX (Model 52721), 6U VPX (Models 57721 and 58721 dual density), XMC module (Model 71720), x8 PCIe (Model 78721), AMC (Model 56721), 6U cPCI (Models 72721 and 74721 dual density), and 3U cPCI (Model 73721).

GateXpress for FPGA-PCIe Configuration Management

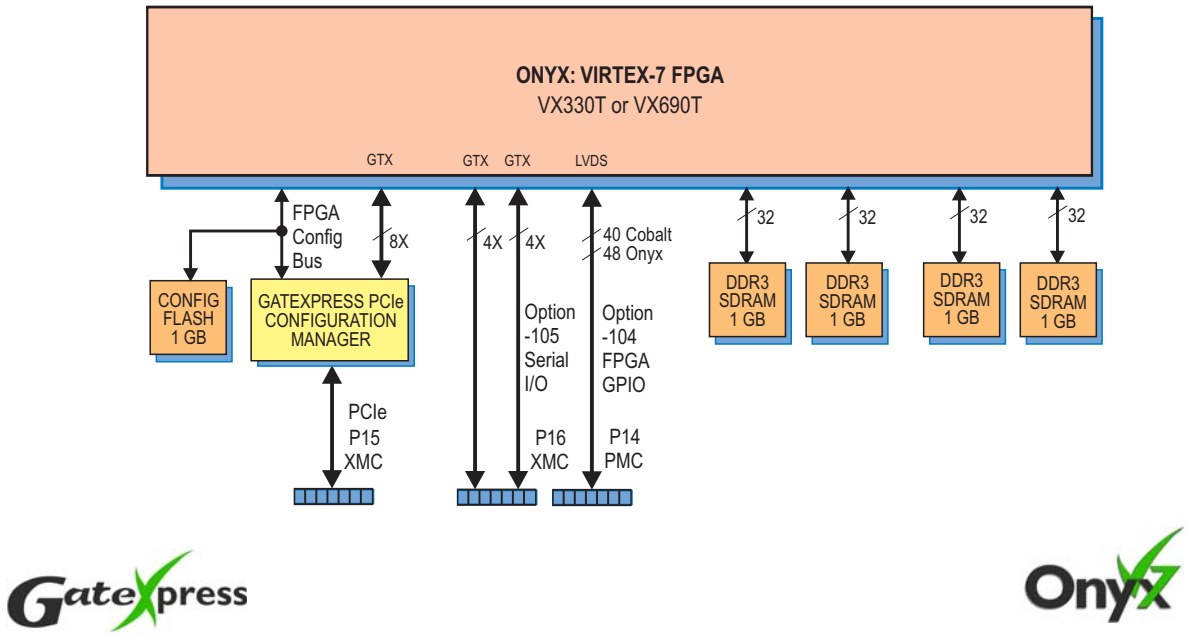


Figure 34

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

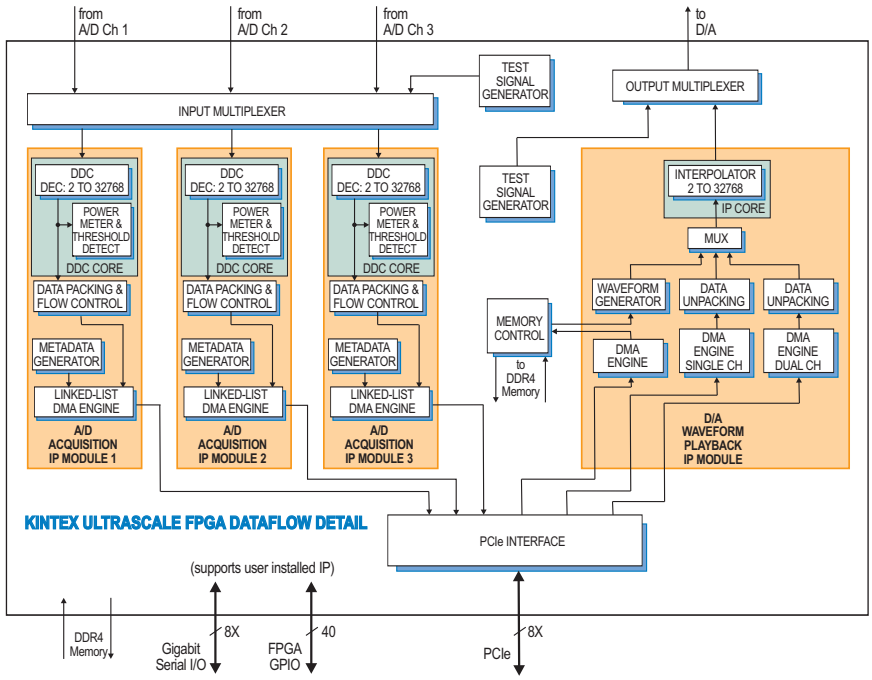
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

3-Channel 200 MHz A/D, DDCs, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Kintex UltraScale FPGA

Model 53821- 3U VPX



Model 53821
COTS and Rugged

JADE
NAVIGATOR
Design Suite

Figure 35

Model 53821 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53821 is a 3-channel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multi-board clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The 53821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer. Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53821 to operate as a complete turnkey solution for many applications.

Versions of the 53821 are also available as an XMC module (Model 71821), x8 PCIe board (Model 78821), 3U VPX (Model 52821), 6U VPX (Models 57821 and 58821 dual density), AMC (Model 56821), 6U cPCI (Models 72821 and 74821 dual density), and 3U cPCI (Model 73821).

Pentek Navigator

NAVIGATOR Design Suite

XILINX VIVADO ALLIANCE PROGRAM CERTIFIED

JADE

Figure 36

Pentek's Navigator Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, ***and*** software to control the FPGA hardware from a host computer.

Even when "turnkey" solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek's Jade™ architecture and provide a better solution to the complex task of IP and software creation.

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade data acquisition and processing board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design. Each Navigator/Jade design includes User Blocks in the data-flow path, ideal for inserting custom processing IP.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP. In addition to the IP specific to the supported Jade board, Navigator also includes processing blocks for some of the most commonly used algorithms. ➤

Pentek Navigator

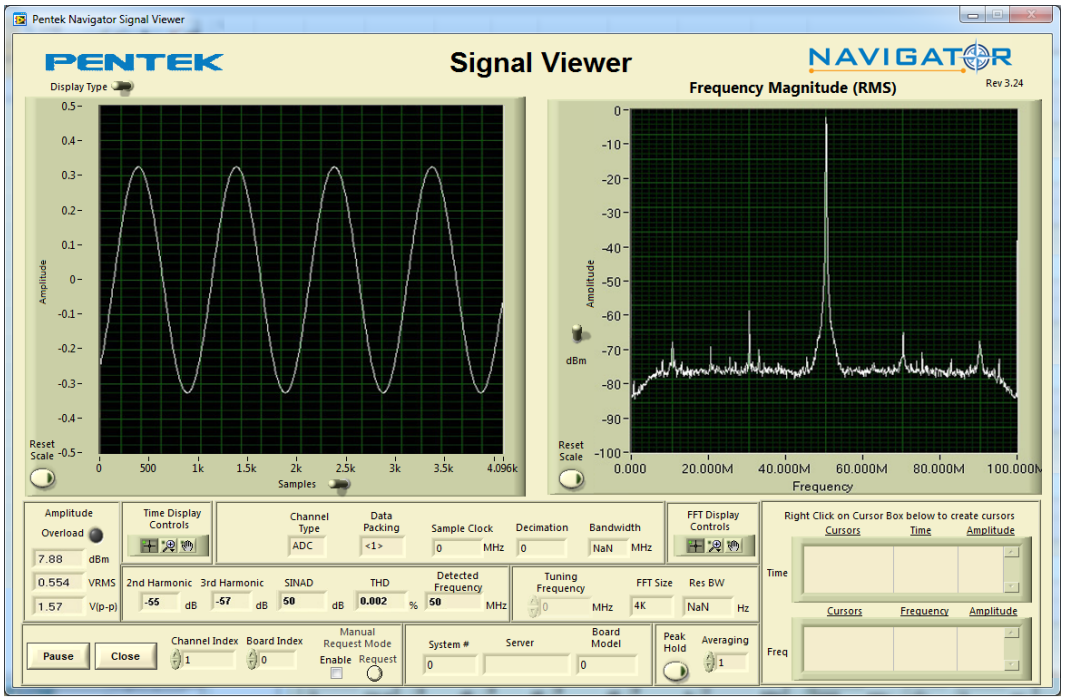


Figure 37

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.

Dual-Channel 34-Signal Adaptive IF Relay, Installed IP Cores, Virtex-6 FPGA

Model 52624 - 3U VPX

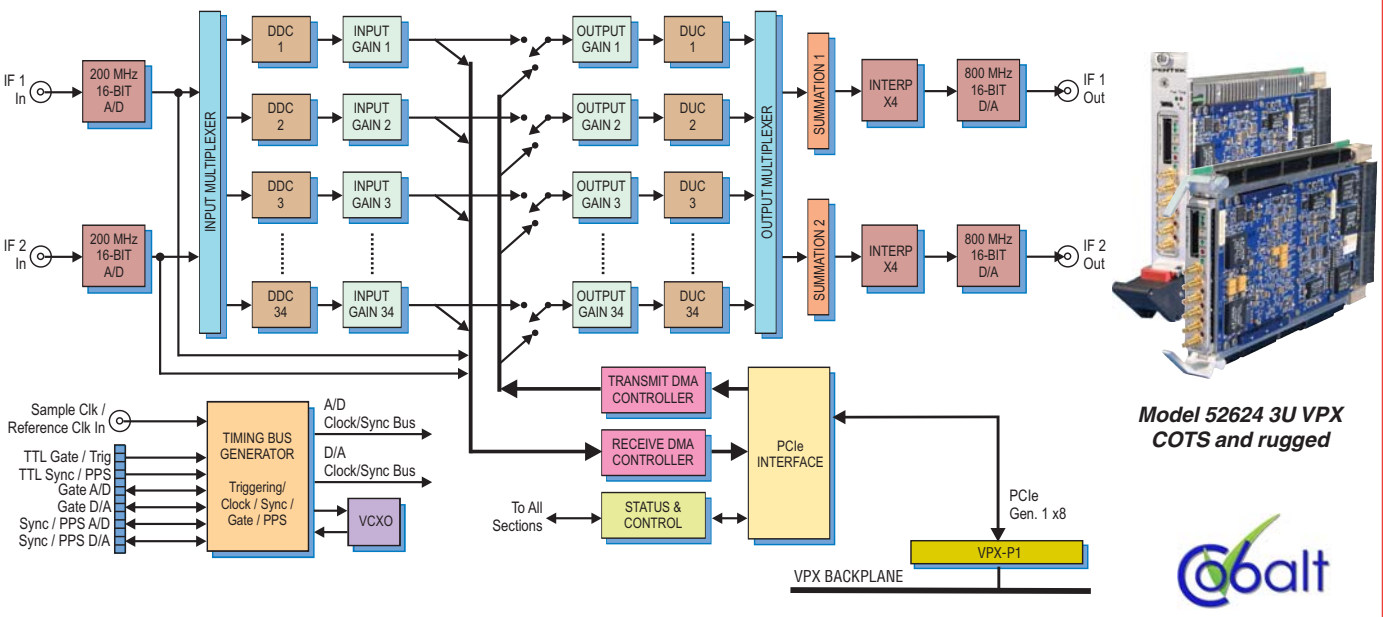


Figure 38

Model 52624 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

The 52624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

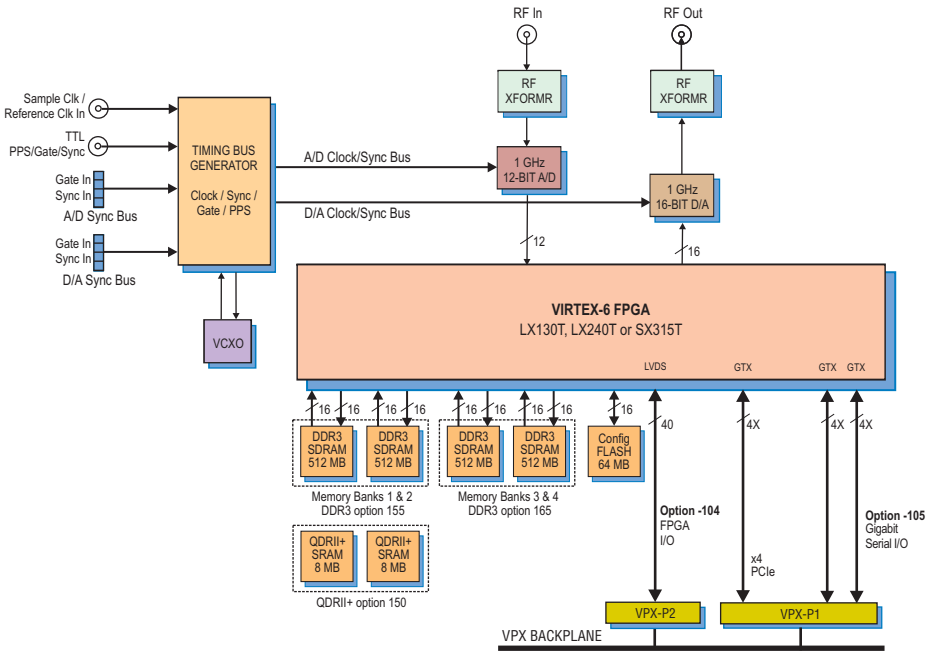
The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay. A PCIe Gen 1 system interface supports control, status and data transfers.

The Model 52624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Versions of the 52624 are also available as a different 3U VPX (Model 53624), 6U VPX (Models 57624 and 58624 dual density), XMC module (Model 71624), an x8 PCIe board (Model 78624), AMC (Model 56624), 6U cPCI (Models 72624 and 74624 dual density), and 3U cPCI (Model 73624).

1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA

Model 52630 - 3U VPX



Model 52630 3U VPX
COTS and rugged

Figure 39

Model 52630 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 52630 includes optional general purpose and gigabit serial card connectors for application- specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

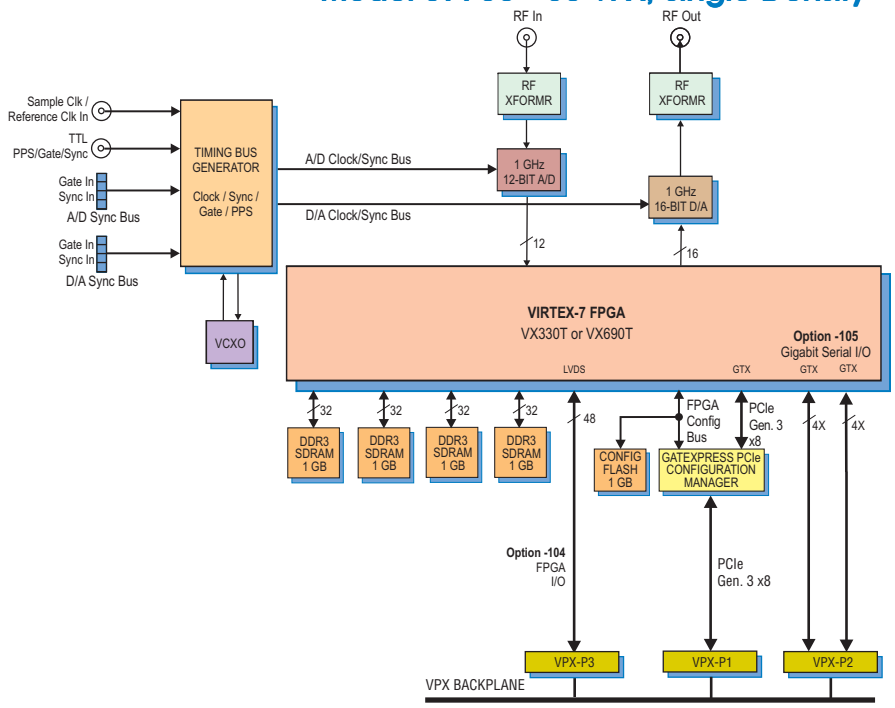
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 52630's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations.

Versions of the 52630 are available as a different 3U VPX (Model 53630), 6U VPX (Models 57630 and 58630 dual density), XMC (Model 71630), x8 PCIe Model 78630) AMC (Model 56630), 6U cPCI (Models 72630 and 74630 dual density), and 3U cPCI (Model 73630).

1 GHz A/D,1 GHz D/A, Virtex-7 FPGA

Model 57730 - 6U VPX, Single Density



Model 57730
6U VPX
single density

Onyx
GateXpress See page 29

Figure 40

Model 57730 is a member of the Onyx family of high-performance 6U VPX boards based on the Xilinx Virtex-7 FPGAs. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP. It includes a 1 GHz A/D, a 1 GHz D/A converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57730 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Onyx architecture features two Virtex-7 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as containers for data-processing applications where each function exists as an intellectual property (IP) module.

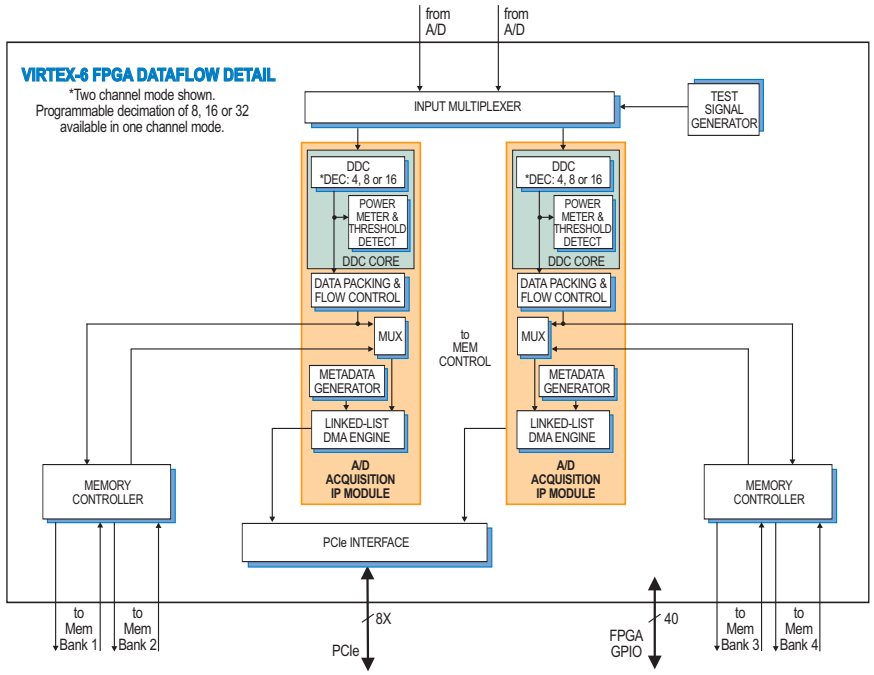
Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 57730 factory-installed functions include one A/D acquisition and one D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 57730 to operate without the need to develop any FPGA IP.

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer coupling into TI ADS5400 1 GHz, 12-bit A/D converter. The digital outputs are delivered into the Virtex-7 FPGAs for signal processing.

Versions of the 57730 are available as 6U VPX (Model 58730 dual density), 3U VPX (Models 52730 and 53730), XMC (Model 71730), x8 PCIe (Model 78730), AMC (Model 56730), 6U cPCI (Models 72730 and 74730 with dual density), and 3U cPCI (Model 73730).

1- Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-6 FPGA

Model 53641 - 3U VPX



Model 53641 3U VPX
COTS and rugged

Figure 41

Model 53641 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A very high-speed data converter based on the Model 53641 described in the previous page, it includes additional factory-installed IP cores to enhance the performance of the 56640 and address the requirements of many applications.

The 53641 factory-installed functions include an A/D acquisition IP module. In addition, within the FPGA is a powerful factory-installed DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Versions of the 53641 are available as a different 3U VPX (Model 52641), 6U VPX (Models 57641and 58641 dual density), XMC (Model 71641), x8 PCIe Model 78641) AMC (Model 56641), 6U cPCI (Models 72641 and 74641 dual density), and 3U cPCI (Model 73641).

1- Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-7 FPGA

Model 53741 - 3U VPX

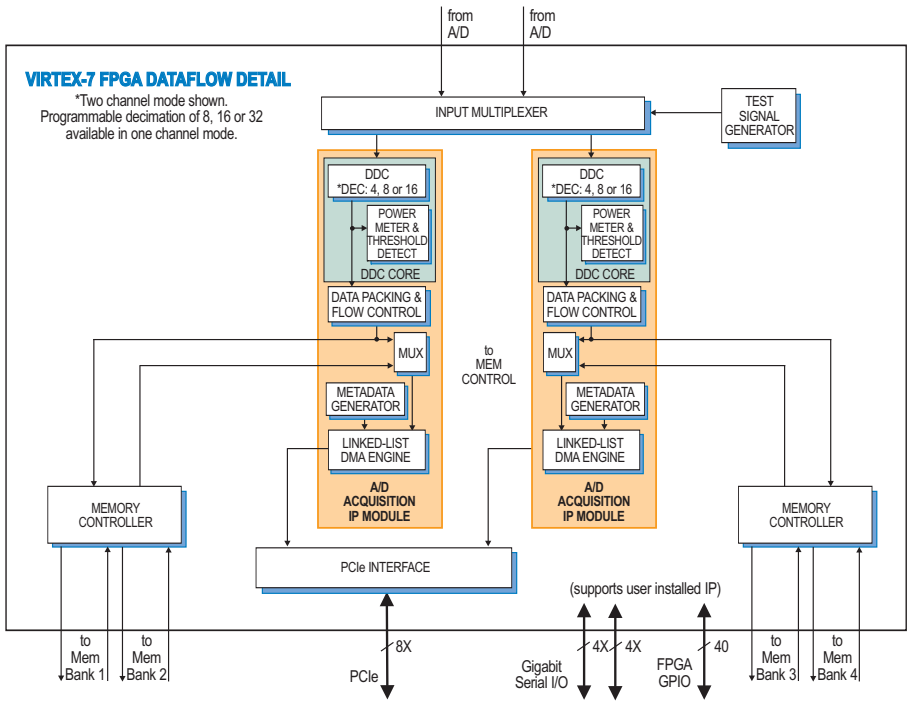


Figure 42

Model 53741 3U VPX
COTS and rugged

Onyx
GateXpress

See page 29

Model 53741 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

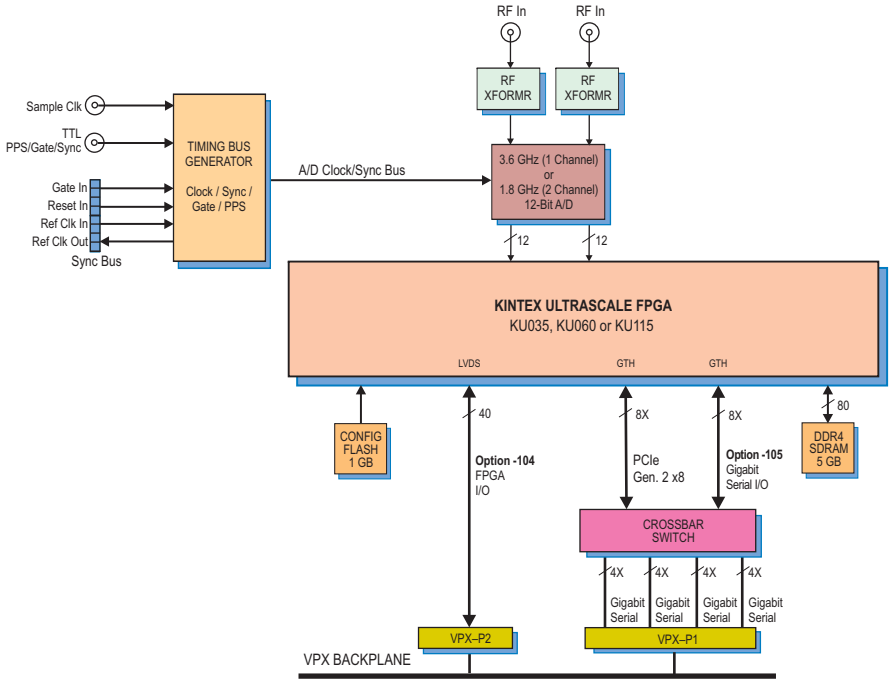
The 53741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter.

The DDC core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation. In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s. In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

Versions of the 53741 are available as a different 3U VPX (Model 52741), 6U VPX (Models 57741and 58741 dual density), XMC (Model 71741), x8 PCIe Model 78741) AMC (Model 56741), 6U cPCI (Models 72741 and 74741 dual density), and 3U cPCI (Model 73741).

1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA

Model 53841 - 3U VPX



Model 53841 3U VPX COTS and Rugged

JADE NAVIGATOR Design Suite

Figure 43

Model 53841 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53841 is a high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

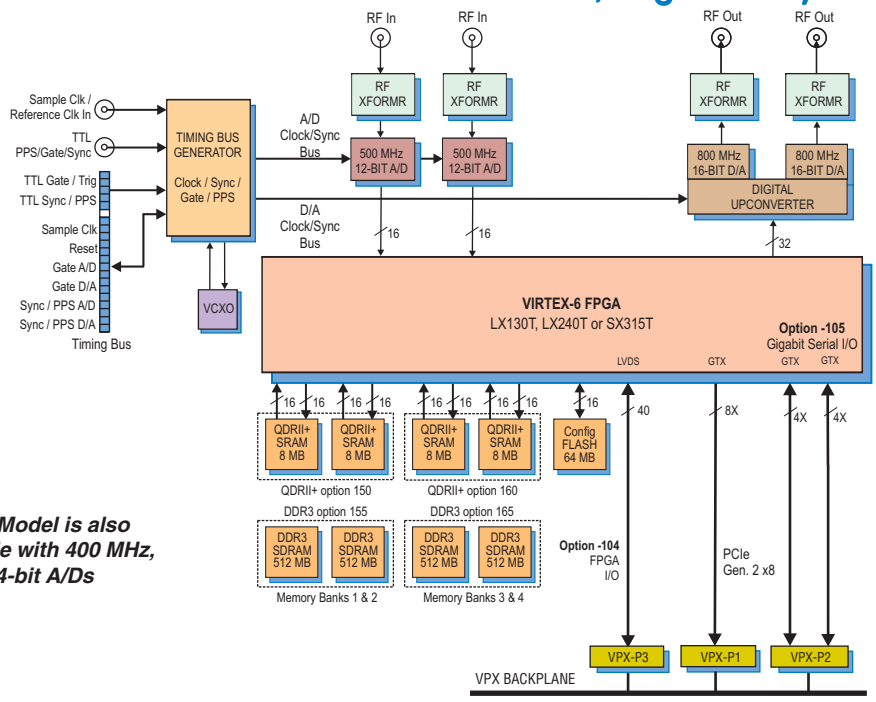
It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Versions of the 53841 are also available as an XMC module (Model 71841), 3U VPX (Model 52841), 6U VPX (Models 57841 and 58841 with dual density), AMC (Model 56841), 6U cPCI (Models 72841 and 74841 with dual density), and 3U cPCI (Model 73841).

2-Channel 500 MHz A/D, DUCs, 2-Channel 800 MHz D/A, Virtex-6 FPGAs

Model 57650 - 6U VPX, Single Density



This Model is also available with 400 MHz, 14-bit A/Ds

Model 57650 6U VPX single density

Figure 44

Model 57650 is a member of the Cobalt family of high-performance 6U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP. The 57650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/A and four banks of memory. It features built-in support for PCI Express over the 6U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as containers for data-processing applications where each function exists as an intellectual property (IP) module.

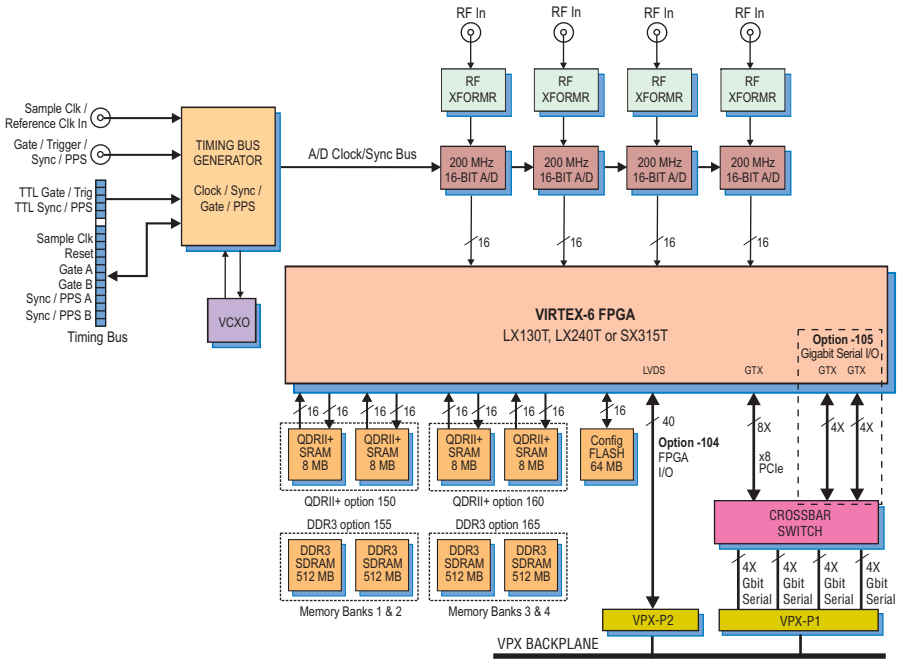
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 57650 factory-installed functions include A/D acquisition and D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 57650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations of these.

Versions of the 57650 are available as another 6U VPX (Model 58650 double density), 3U VPX (Models 52650 and 53650), XMC module (Model 71650), x8 PCIe (Model 78650), AMC (Model 56650), 6U cPCI (Models 72650 and 74650 dual density), and 3U cPCI (Model 73650).

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

Model 53660 - 3U VPX



Model 53660 3U VPX
COTS and rugged

Figure 45

Model 53660 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 53660 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

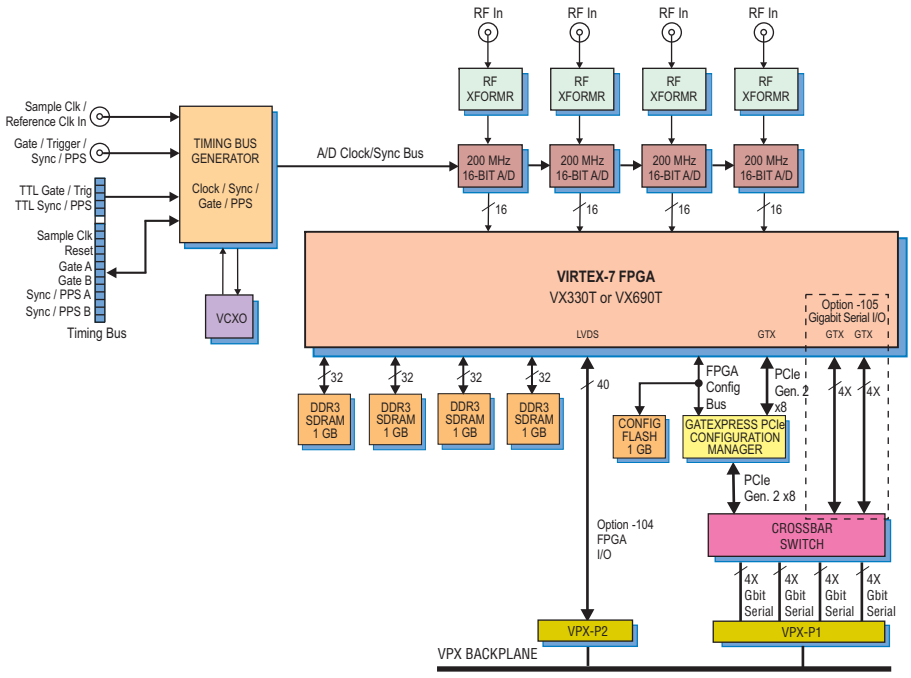
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 53660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 53660 are available as another 3U VPX (Model 52660), 6U VPX (Models 57660 and 58660 dual density), XMC (Model 71660), x8PCIe (Model 78660), AMC (Model 56660), 6U cPCI (Models 72660 and 74660 with dual density), and 3U cPCI (Model 73660).

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA

Model 53760 - 3U VPX



Model 53760 3U VPX
COTS and rugged

See page 29

Figure 46

Model 53760 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the flagship family of Virtex-7 FPGA from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

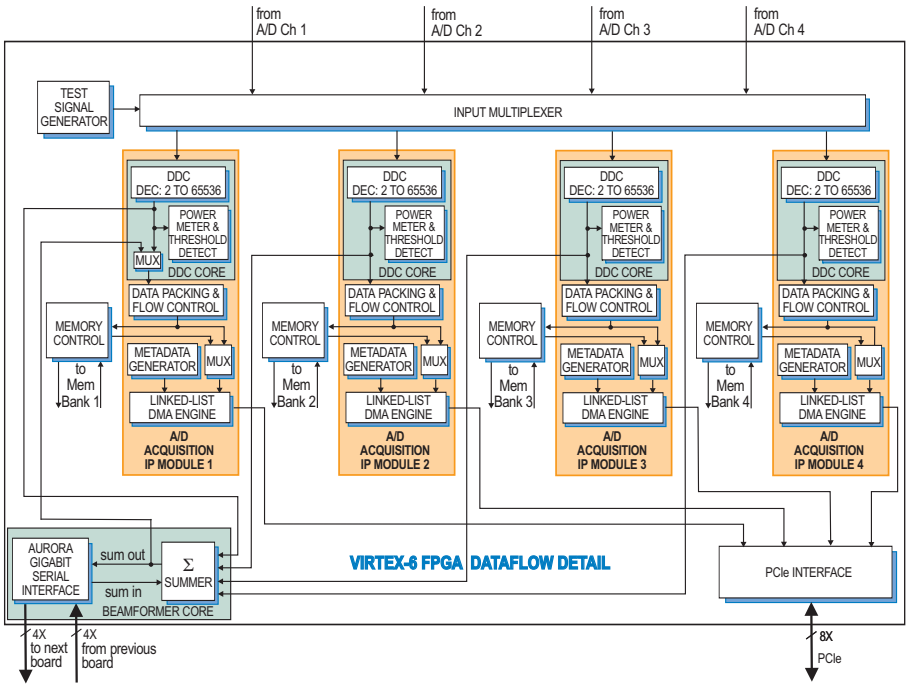
Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data tranfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

The 53760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 53760 are available as a different 3U VPX (Model 52760), 6U VPX (Models 57760 and 58760 dual density), XMC (Model 71760), x8 PCIe (Model 78760), AMC (Model 56760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).

4-Channel 200 MHz 16-bit A/D with Installed DDC and Beamforming Cores, Virtex-6 FPGA

Model 53661 - 3U VPX



Model 53661 3U VPX COTs and rugged

Figure 47

Model 53661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 53660 described earlier, it includes factory-installed IP cores to enhance the performance of the 53660 and address the requirements of many applications.

The 53661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

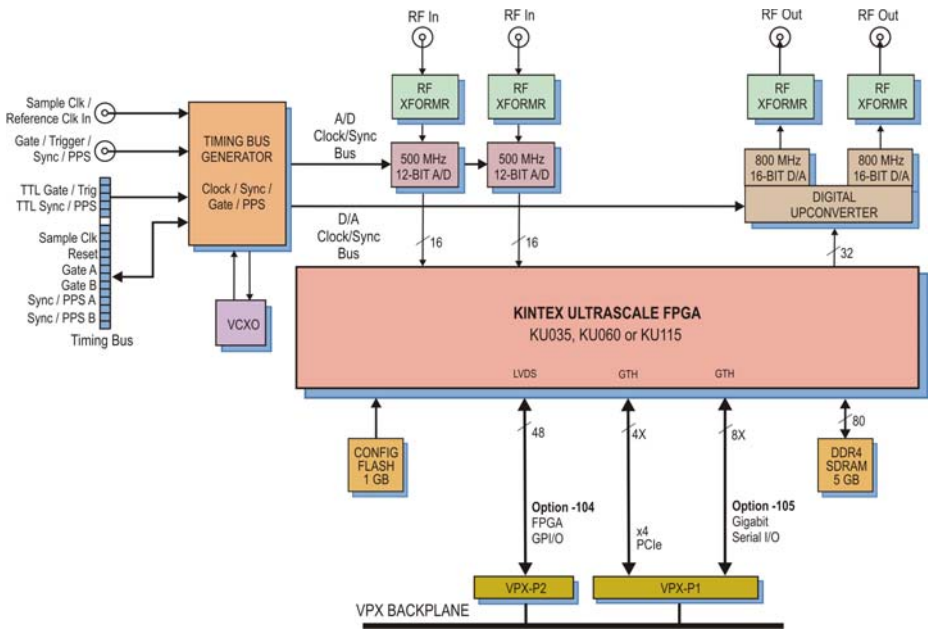
The 53661 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 53661's can be chained together via the built-in Xilinx Aurora gigabit serial interface. More on Beamforming Application, page 82.

Versions of the 53661 are available as another 3U VPX (Model 52661), 6U VPX (Models 57661 and 58661 dual density), XMC (Model 71661), x8 PCIe (Model 78661), AMC (Model 56661), 6U cPCI (Models 72661 and 74661 dual density), and 3U cPCI (Model 73661).

2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Kintex UltraScale FPGA

Model 52851 - 3U VPX



Model 52851 3U VPX COTS and Rugged

JADE NAVIGATOR Design Suite

Figure 48

Model 52851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new stream-lined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52851 is a 2-channel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

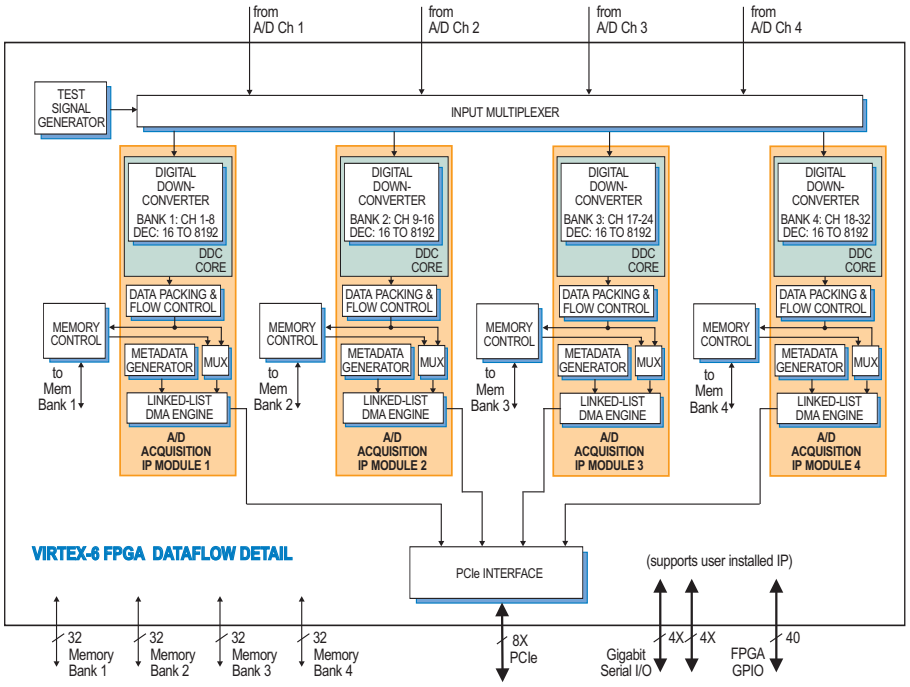
The 52851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52851 to operate as a complete turnkey solution for many applications.

Versions of the 52851 are also available as a 3U VPX (Model 53851), 6U VPX (Models 57851 and 58851 dual density), XMC module (Model 71851), a PCIe board (Model 78851), AMC (Model 56851), 6U cPCI (Models 72851 and 74851 dual density), and 3U cPCI (Model 73851).

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 53662 - 3U VPX



Model 53662 3U VPX
COTs and rugged

Figure 49

Model 53662 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. Based on the Model 53660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 53662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 53662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 53662 are available as another 3U VPX (Model 52662), 6U VPX (Models 57662 and 58662 dual density), XMC (Model 71662), x8 PCIe (Model 78662), AMC (Model 56662), 6U cPCI (Models 72662 and 74662 dual density), and 3U cPCI (Model 73662).

1100-Channel GSM Channelizer with Quad A/D, Virtex-6 FPGA

Model 53663 - 3U VPX

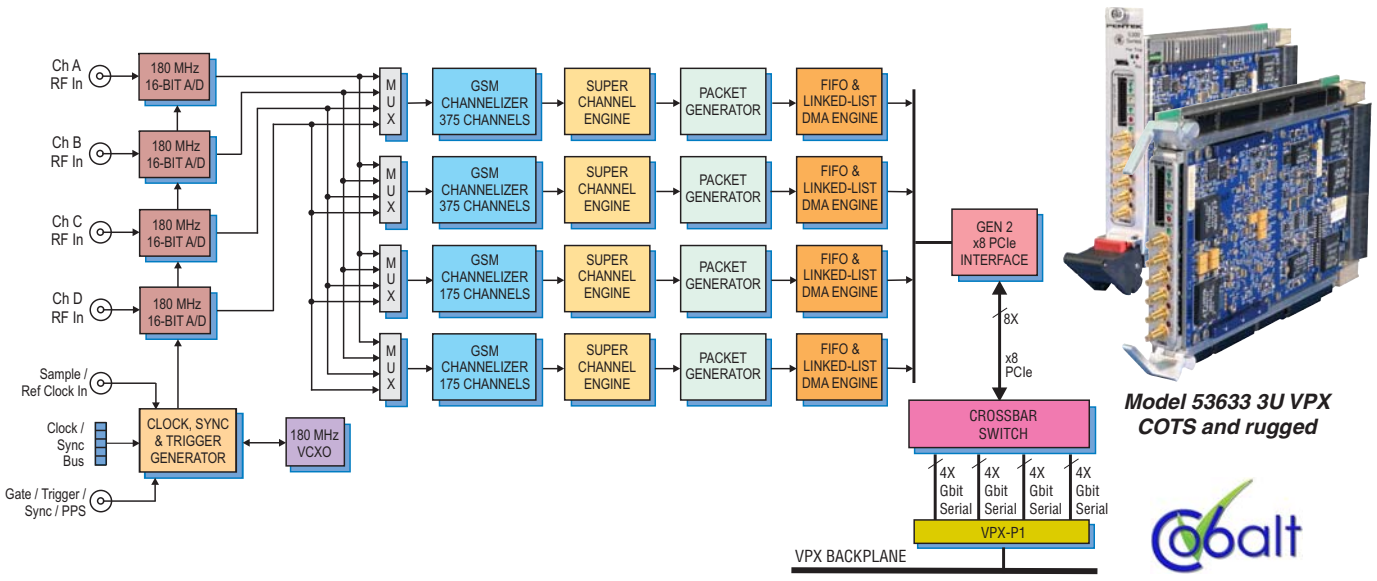


Figure 50

The Model 53663 accepts four analog inputs from an external analog RF tuner, such as the Pentek Model 8111, where the GSM RF bands are downconverted to an IF frequency. These IF signals are then digitized by four A/D converters and routed to four channelizer banks, which perform digital downconversion of all GSM channels to baseband. Two of the banks handle 175 channels for the lower GSM transmit/receive bands and two more banks handle 375 channels for the upper bands. The DDC channels within each bank are equally spaced at 200 kHz.

Each DDC output is resampled to a 4x symbol rate of 1.08333 MHz to simplify symbol recovery. Every four DDC outputs are combined into a frequency-division "super-channel" that allows transmission of all 1100 channels across the PCIe Gen. 2 x4 interface. The GSM channelizer IP core is supported with factory-installed FPGA functions including packet formation, time stamping, four DMA controllers, gating and triggering.

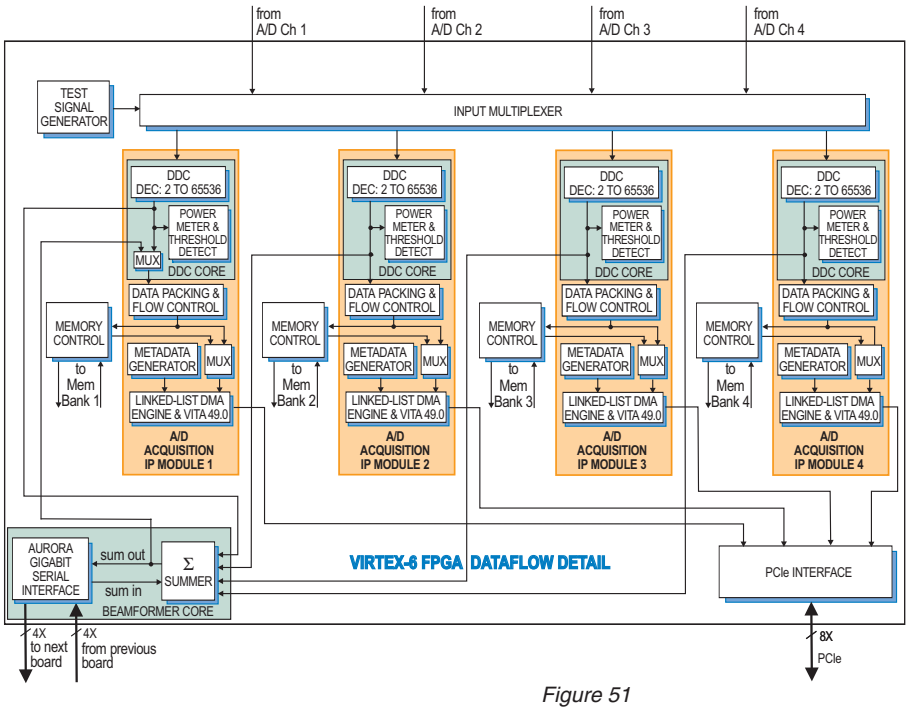
Super-channel packets are formed by appending enabled super-channel samples sequentially from each bank. Once complete, a unique super-channel packet header is inserted at the beginning of each packet for identification. The header contains a time stamp, a sequential packet count, the number of enabled super-channels, the DMA channel identifier, and other information.

The 53663 is ideal for mobile monitoring systems that must capture some or all of the 1100 uplink and downlink signals in both upper and lower GSM bands. This full-global system for mobile communications spectrum monitoring targets homeland security, government and military applications.

Versions of the 53663 are available as another 3U VPX (Model 52663), 6U VPX (Models 57663 and 58663 dual density), XMC (Model 71663), x8 PCIe (Model 78663), AMC (Model 56663), 6U cPCI (Models 72663 and 74663 dual density), and 3U cPCI (Model 73663).

4-Channel 200 MHz 16-bit A/D with Installed DDC and VITA 49.0 IP Cores, Virtex-6 FPGA

Model 53664 - 3U VPX



Model 53664 3U VPX
COTS & Rugged

Figure 51

Model 53664 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 53660 described previously, it includes a programmable DDC and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 53664 PCIe output supports fully the VITA 49.0 VITA Radio Transport (VRT)Standard described on page 14.

The 53664 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

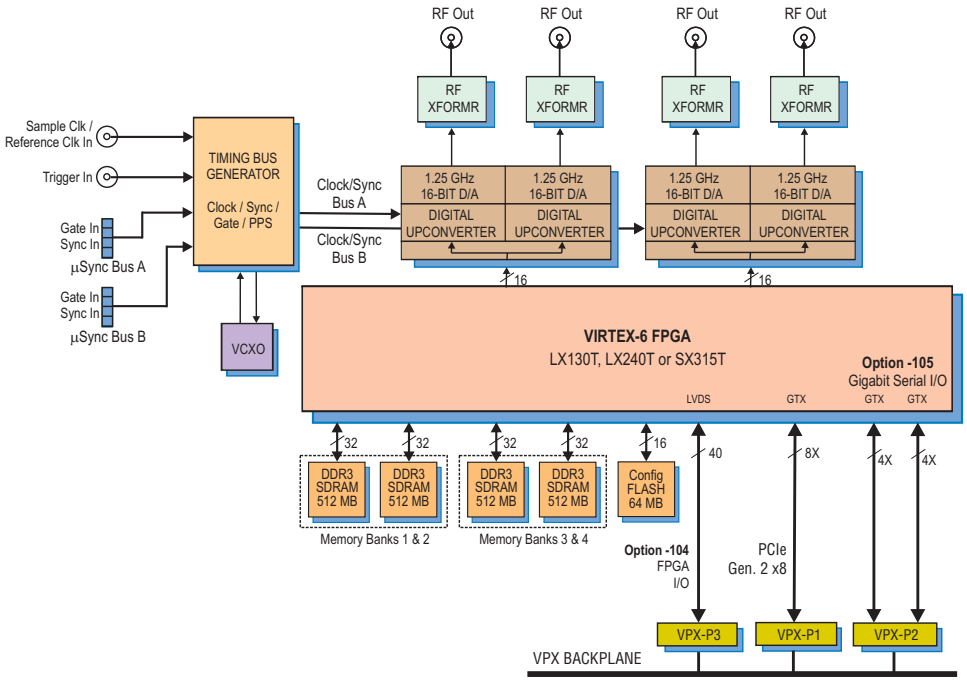
The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically, each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver. The 53664 supports fully the VITA-49.0 specification.

Versions of the 53664 are also available as a different 3U VPX (Model 52664), 6U VPX (Models 57664 and 58664 dual density), XMC (Model 71664), x8 PCIe (Model 78664), AMC (Model 56664), 6U cPCI (Models 7266 and 74664 dual density), and 3U cPCI (Model 73664).

4-Channel 1.25 GHz D/A with DUCs, Virtex-6 FPGA

Model 57670 - 6U VPX, Single Density



Model 57670
6U VPX
single density

Figure 52

Model 57670 is a member of the Cobalt family of high-performance 6U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 57670 includes a front panel general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The Model 57670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 57670 to operate as a turnkey solution without the need to develop FPGA IP.

Versions of the 57670 are also available as 6U VPX (Model 58670 dual density), 3U VPX (Models 53670 and 52670), XMC (Model 71670), PCIe (Model 78670),AMC (Model 56670), 6U cPCI (Models 72670 and 74670 dual density), and 3U cPCI (Model 73670).

4-or 8-Channel 200 MHz 16-bit A/D with Installed IP Cores, Kintex Ultrascale FPGA

Models 57861 and 58861 - 6U VPX

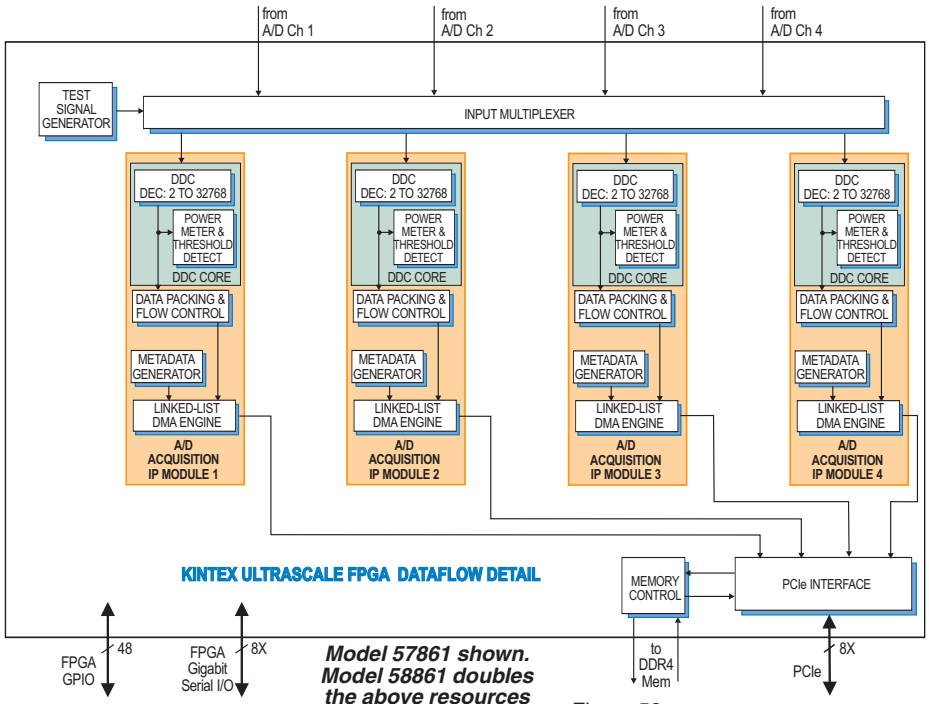


Figure 53

Model 78861
6U VPX
Dual Density

JADE NAVIGATOR Design Suite

Models 57861 and 58861 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a 6U VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

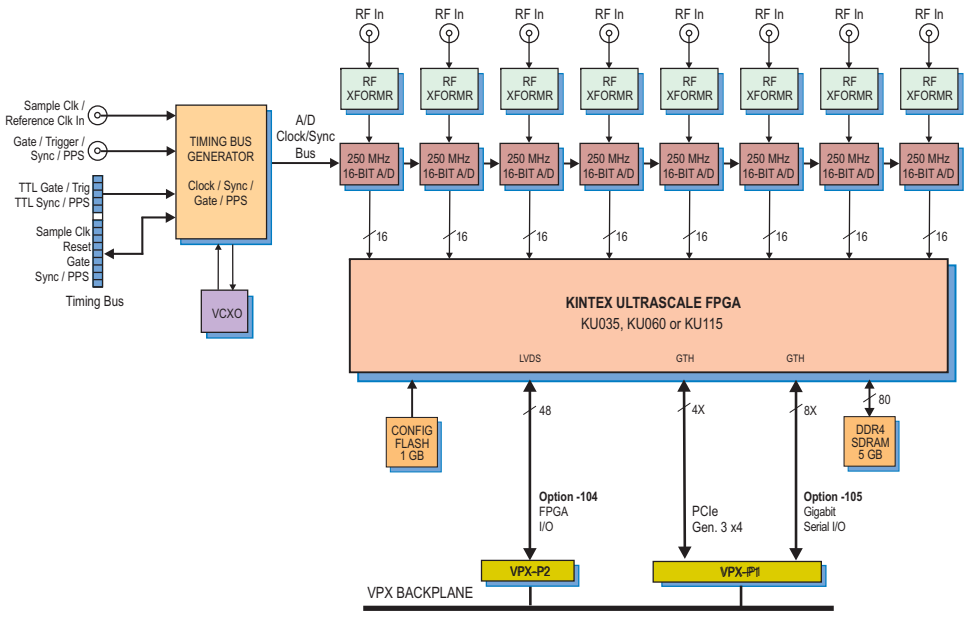
These models include four or eight A/Ds, complete multiboard clock and sync sections, and large DDR4 memories. Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Models 57861 and dual density Model 58861 are 6U VPX boards; also available are an XMC (Model 71861), x8 PCIe (Model 78861), AMC (Model 56861); 3U VPX (Models 52861 and 53861), 6U cPCI (Models 72861 and 74861 dual density), and 3U cPCI (Model 73861).

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA

Model 52131 - 3U VPX



Model 52131 3U VPX COTS and Rugged

JADE NAVIGATOR Design Suite

Figure 66

Model 52131 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52131 is a multichannel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

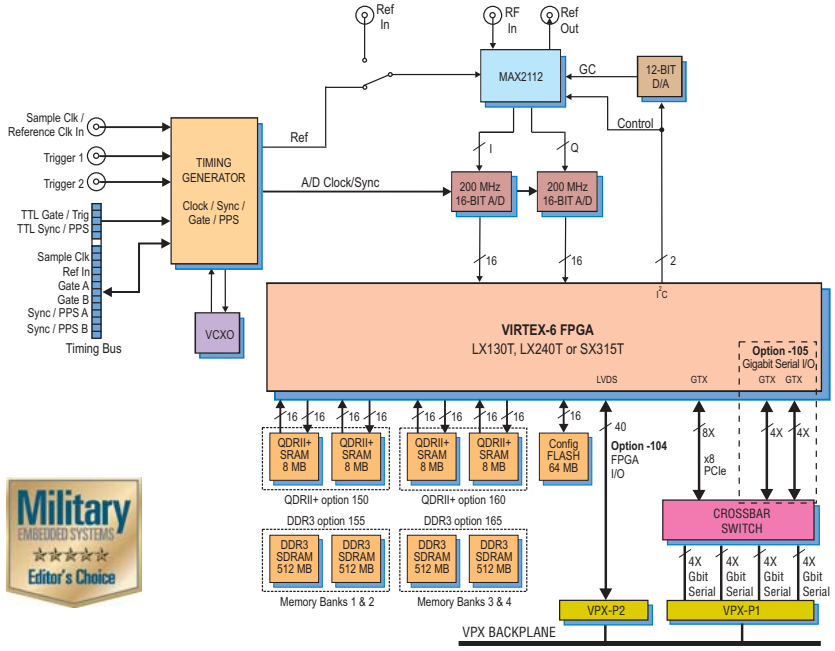
It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer. Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52131 to operate as a complete turnkey solution for many applications.

Versions of the 52131 are available as an XMC (Model 71131) an x8 PCIe board (Model 78131), 3U VPX (Model 53131), 6U VPX (Models 57131 and 58131 (dual density), AMC (Model 56131), 6U cPCI (Models 72131 and 74131 with dual density), and 3U cPCI (Model 73131).

L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA

Model 53690 - 3U VPX



Model 53690 3U VPX COTS and rugged

Figure 54

Model 53690 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

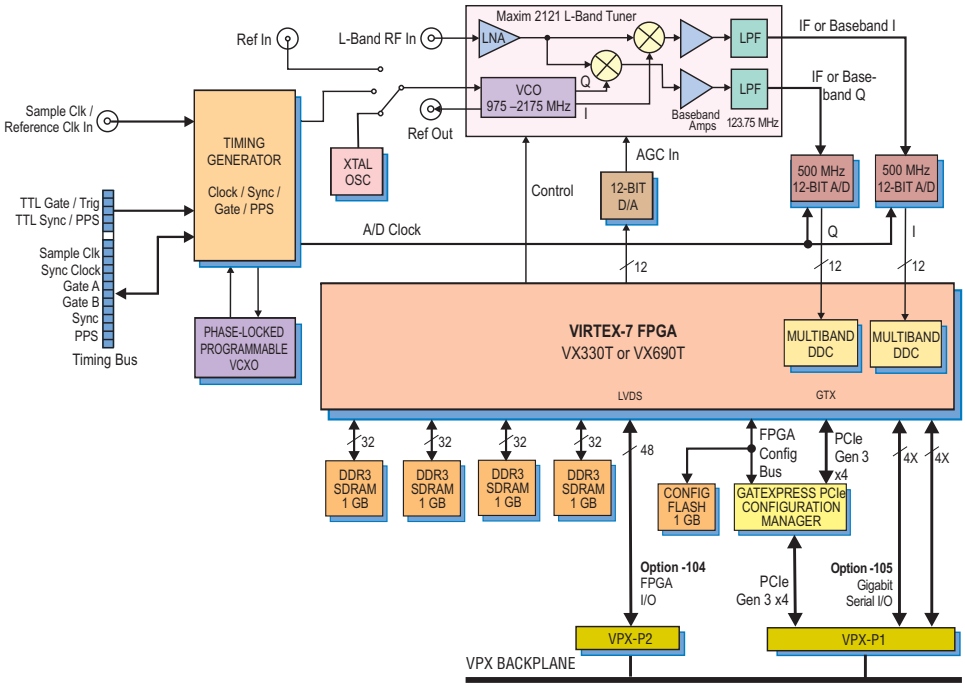
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters and variable-gain baseband amplifiers. See an L-Band Application on page 81.

Versions of the 53690 are available as a different 3U VPX (Model 52690), 6U VPX (Models 57690 and 58690 dual density), XMC (Model 71690), an x8 PCI (Model 78690), AMC (Model 56690), 6U cPCI (Models 72690 and 74690 dual density), and 3U cPCI (Model 73690).

L-Band RF Tuner with 2-Channel 500 MHz A/D and Virtex-7 FPGA

Model 52791 - 3U VPX



Model 52691 3U VPX COTS and rugged

Onyx GateXpress

See page 29

Figure 55

Model 52791 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to suport factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

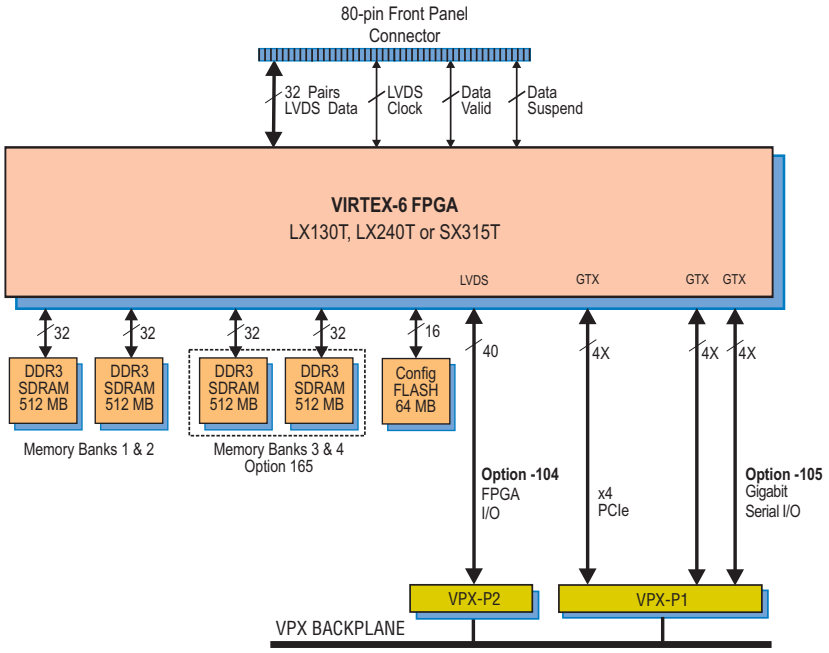
The 52791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

Versions of the 52791 are available as a different 3U VPX (Model 53791), 6U VPX (Models 57791 and 58791 dual density), XMC (Model 71791), an x8 PCI (Model 78791), AMC (Model 56791), 6U cPCI (Models 72791 and 74791 dual density), and 3U cPCI (Model 73791).

LVDS Digital I/O with Virtex-6 FPGA

Model 52610 - 3U VPX



Model 52610 3U VPX
COTS & Rugged

Figure 56

Model 52610 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution.

In addition to supporting PCI Express as a native interface, the Model 52610 includes a general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The 52610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

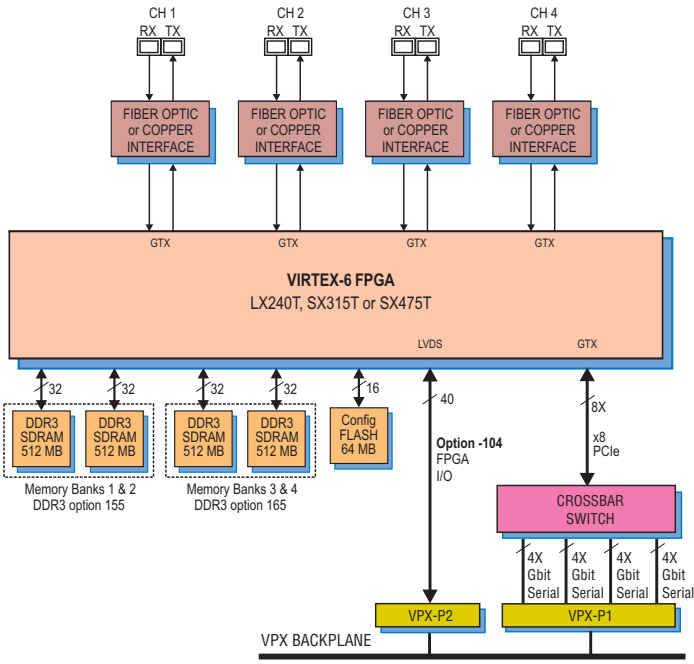
IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The Model 52610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Versions of the 52610 are also available as a different 3U VPX (Model 53610), 6U VPX (Models 57610 and 58610 dual density), XMC (Model 71610), x8 PCIe (Model 78610), AMC (Model 56610), 6U cPCI (Models 72610 and 74610 dual density), and 3U cPCI (Model 73610).

Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA

Model 53611 - 3U VPX



Model 53611 3U VPX
COTS & Rugged

Figure 57

Model 53611 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 53611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 53611 includes a general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 53611 to operate as a complete turnkey solution without developing FPGA IP.

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop.

Versions of the 53611 are available as a different 3U VPX (Model 52611), 6U VPX (Models 57611 and 58611 dual density), XMC (Model 71611); x8 PCIe (Model 78611), AMC (Model 56611), 6U cPCI (Models 72611 and 74611 dual density), and 3U cPCI (Model 73611).

Virtex-7 Processor and FMC Carrier - FMC

Model 5973 - 3U VPX

Model 5973
FMC

OnyxFX
GateXpress

See page 29

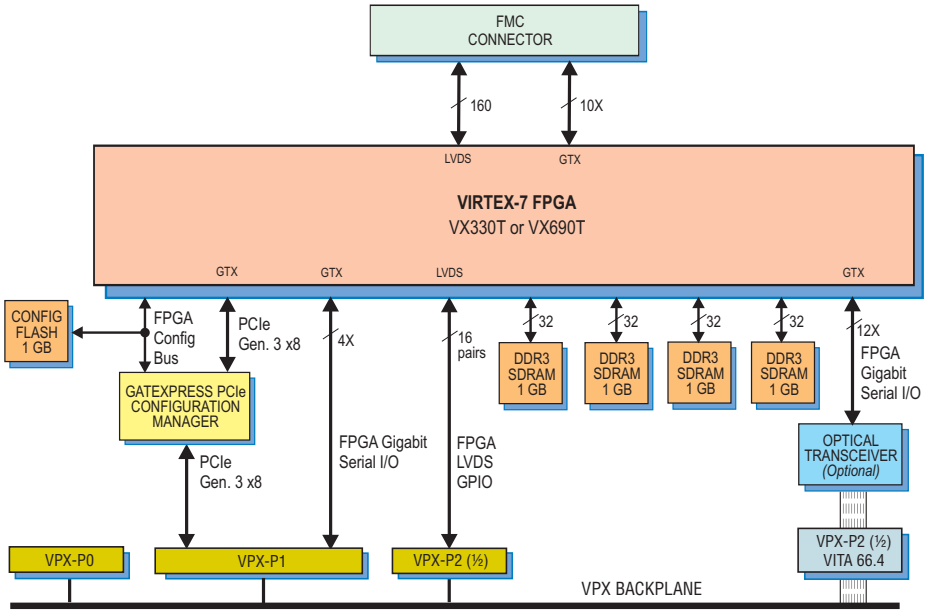


Figure 58

The OnyxFX™ Model 5973 is a high-performance 3U VPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of Flexor® I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A

Model 3312 - FMC

Model 3312
FMC

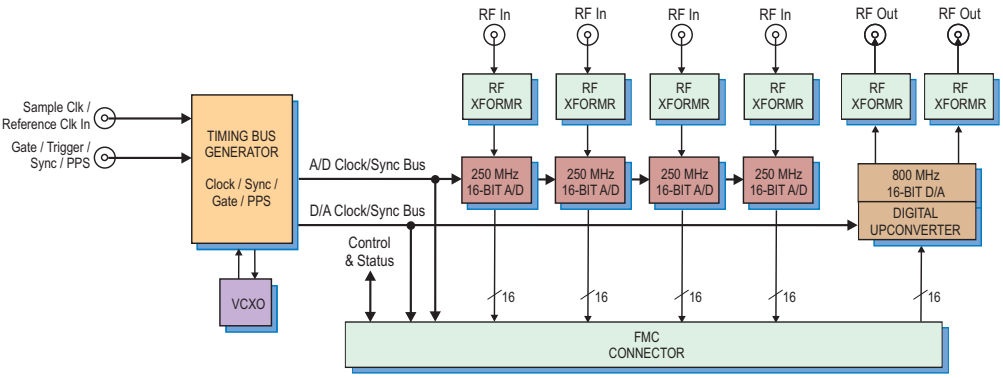


Figure 59

The Flexor Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with the Model 5973 3U VPX carrier, the board-set becomes a turnkey data acquisition and signal generation solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

While users will find the Model 3312 an excellent analog interface to any compatible FMC carrier, the true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 carrier.

With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

When used with the 5973, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

4-Channel 250 MHz A/D, 2-Channel 800 MHz D/A

FlexorSet Model 5973-312 - 3U VPX

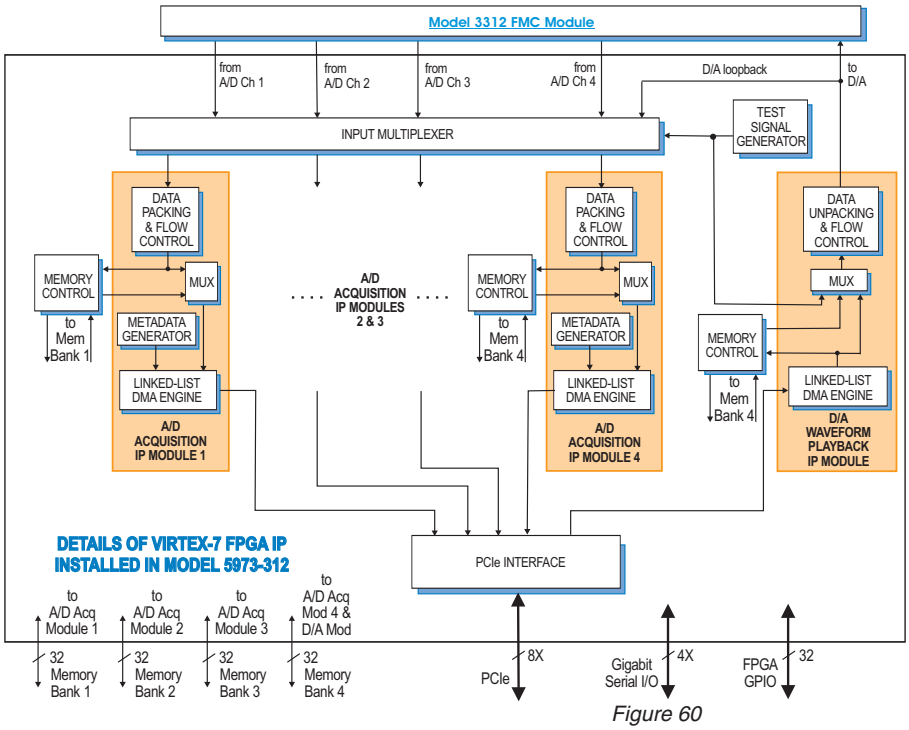


Figure 60

Model 5973-312

GateFlow
ReadyFlow Board Support Package
OnyxFX
GateXpress See page 29

Model 5973-312 is a member of the FlexorSet family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3312 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The FlexorSet includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

This model features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable this model to operate as turnkey solution without the need to develop any FPGA IP.

4-Channel 250 MHz A/D with DDCs, 2-Channel 800 MHz D/A with Extended Interpolation

FlexorSet Model 5973-313 - 3U VPX

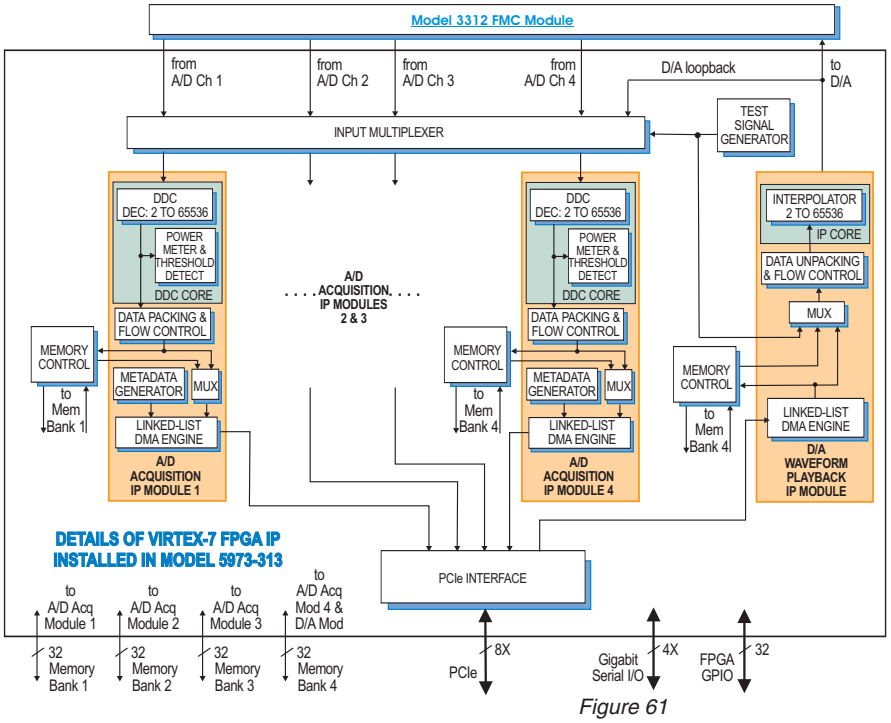


Figure 61

Model 5973-313

GateFlow
ReadyFlow Board Support Package
OnyxFX
GateXpress See page 29

The Model 5973-313 is a member of the FlexorSet family of high-performance 3 U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3312 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with progammable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The FlexorSet includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a programmable DDC core with decimations from 2 to 65,536.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable this model to operate as a turnkey solution without the need to develop any FPGA IP.

8-Channel 250 MHz 16-bit A/D

Model 3316 - FMC

Model 3316
FMC

Flexor

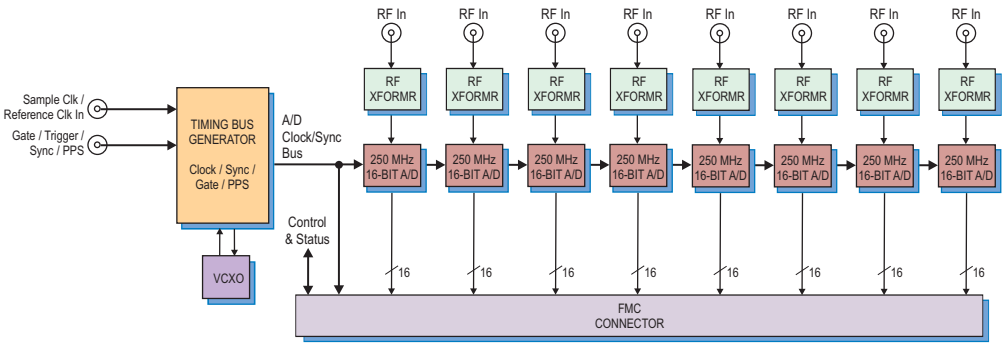


Figure 62

The Flexor Model 3316 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, on-board programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with the Model 5973 3U VPX FMC Carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

The Model 3316 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own FPGA IP for operating the FMC.

While users will find the Model 3316 an excellent analog interface to the VC707, or any compatible FMC carrier, the true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 carrier. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

When the 3316 is installed on the 5973 carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

FlexorSet Model 5973-316 - 3U VPX

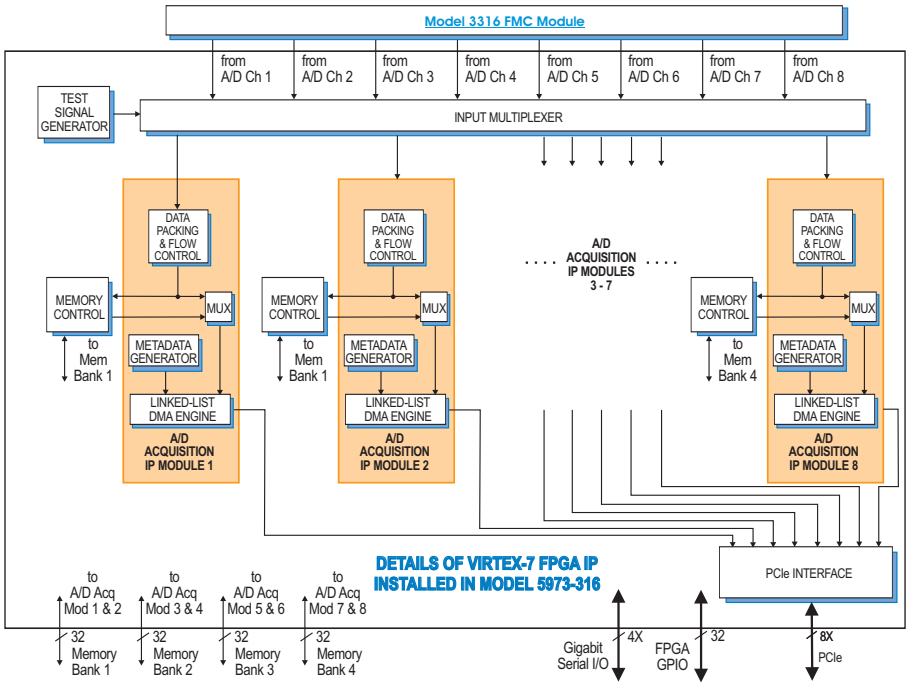


Figure 63

Model 5973-316

GateFlow
ReadyFlow Board Support Package
OnyxFX
GateXpress See page 29

The Model 5973-316 is a member of the FlexorSet family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3316 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

This FlexorSet includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. These functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable this model to operate as turnkey solution without the need to develop any FPGA IP.

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

8-Channel 250 MHz A/D with Digital Downconverters - x8 PCIe

FlexorSet Model 5973-317 - 3U VPX

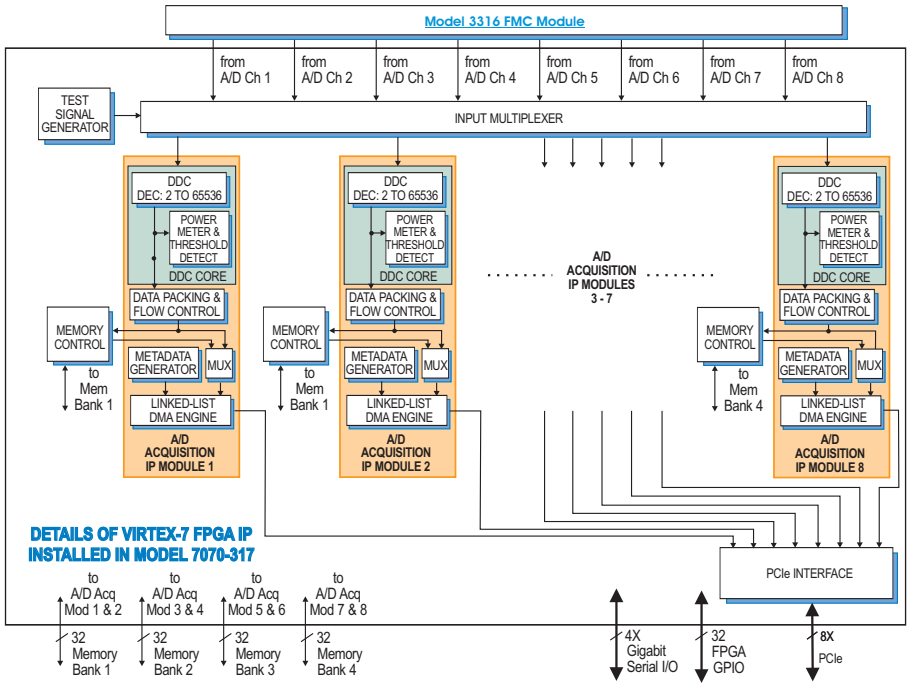


Figure 64

Model 5973-317

GateFlow
ReadyFlow Board Support Package
OnyxFx
GateXpress See page 29

Models 5973-317 is a member of the FlexorSet family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3316 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

Model 3320 - FMC

Model 3320
FMC

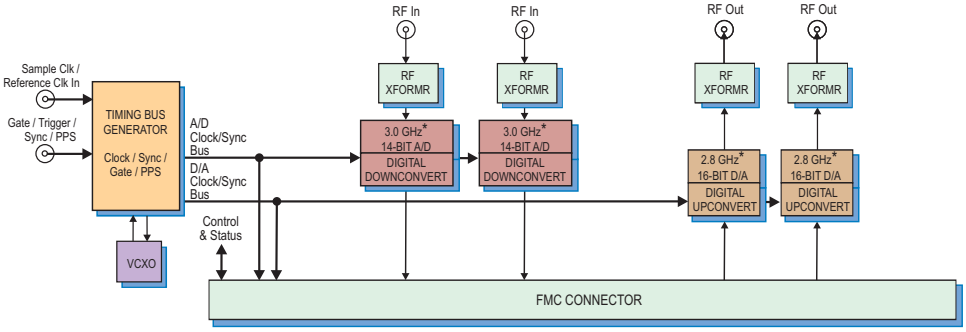


Figure 65

The Flexor Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

When combined with the Model 5973 3U VPX carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 carrier. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

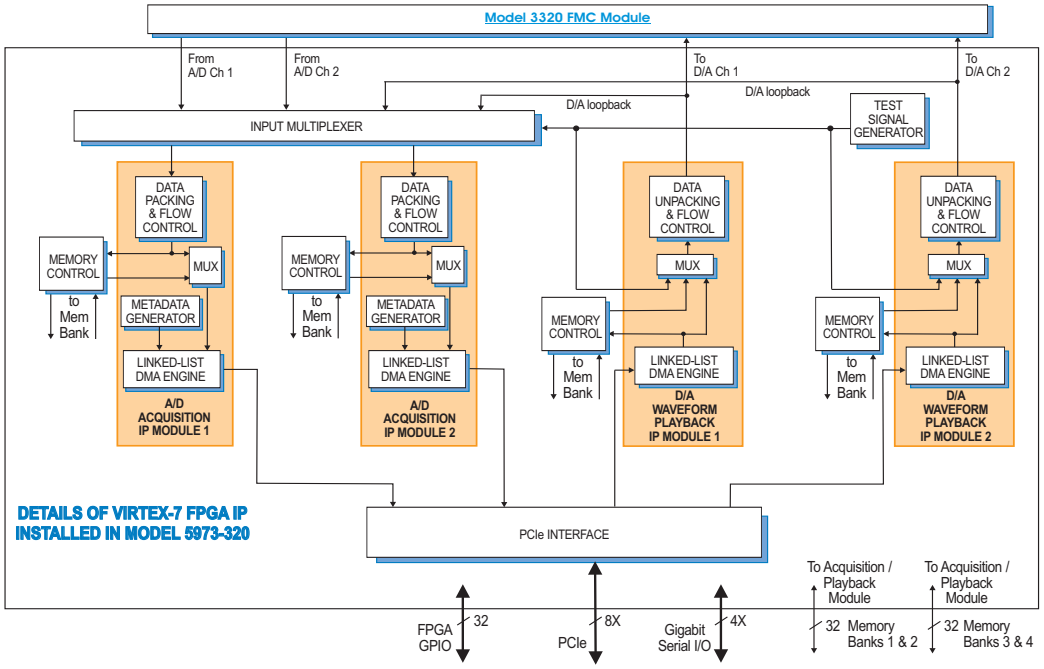
Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital down-converter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications.

With the 3320 installed on the 5973 carrier, the board-set features two A/D Acquisition IP modules for easily capturing and moving data.

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

FlexorSet Model 5973-320 - 3U VPX



Model 5973-320

GateFlow
ReadyFlow Board Support Package
OnyxFX
GateXpress

See page 29

Figure 66

The Model 5973-320 is a member of the FlexorSet family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3320 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA- processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the 5973-320 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP for DDR3 SDRAM memories.

This FlexorSet features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A

Model 3324 - FMC

Model 3324
FMC

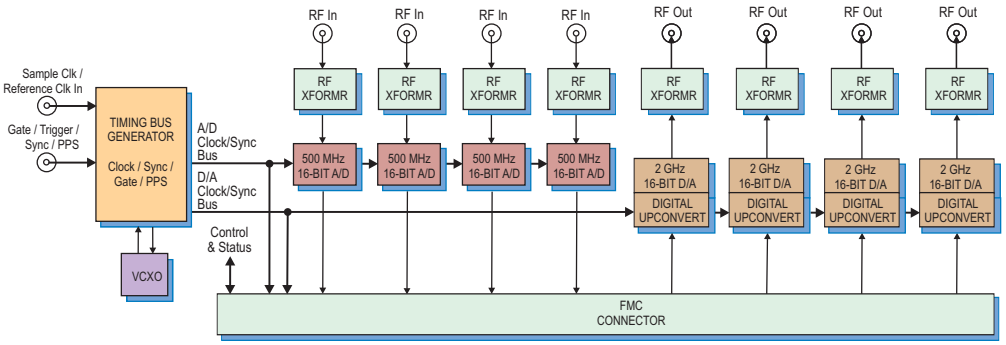


Figure 67

The Flexor Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multi-board synchronization for support of larger high-channel-count systems.

When combined with the Model 5973 3U VPX Carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

The Model 3324 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own IP for operating the FMC.

While users will find the Model 3324 an excellent analog interface to the VC707 or any compatible FMC carrier, the true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 carrier. With factory-installed IP, the board set provides a turnkey data acquisition and signal generation subsystem, eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition engines, D/A waveform playback engines, programmable linked-list DMA engines, and a metadata-packet creator.

The board-set features four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

When used with a Pentek FMC carrier, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A - FMC

Model FlexorSet 5973-324 - 3U VPX

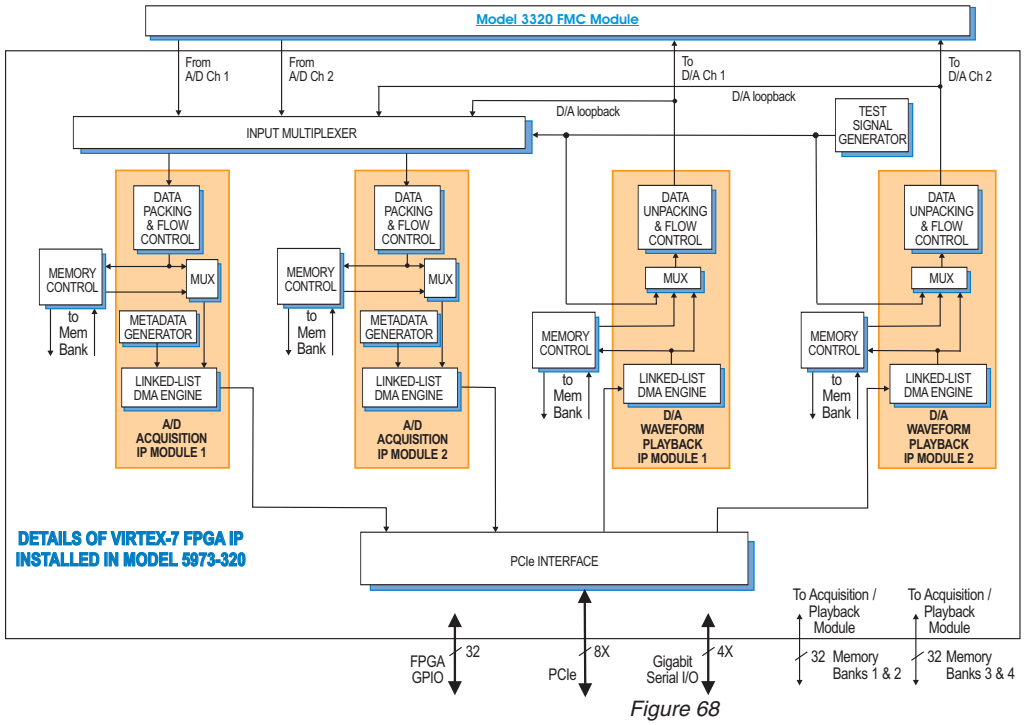


Figure 68

Model 5973-324

GateFlow
ReadyFlow Board Support Package
OnyxFX
GateXpress

See page 29

Model 5973-324 is a member of the FlexorSet family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3324 FMC is factory-installed on the 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The FlexorSet includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, this model includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

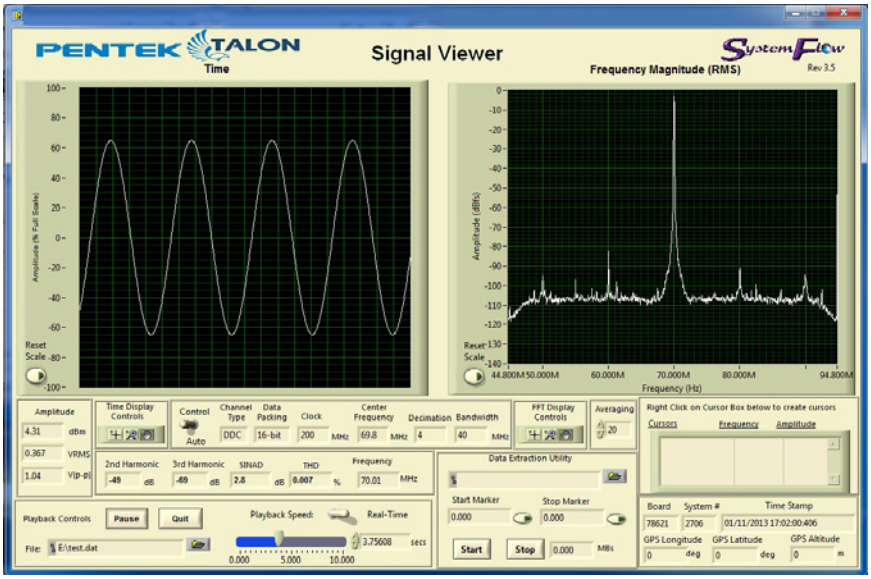
When delivered as an assembled board-set, the 5973-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The FlexorSet features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable this model to operate as turnkey solution without the need to develop any FPGA IP.

PC Development System for PCIe Cobalt, Onyx, Jade and Flexor Boards

Model 8266



Model 8266

SPARK Development Systems

ReadyFlow Board Support Package

Figure 69

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx, Jade and Flexor PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

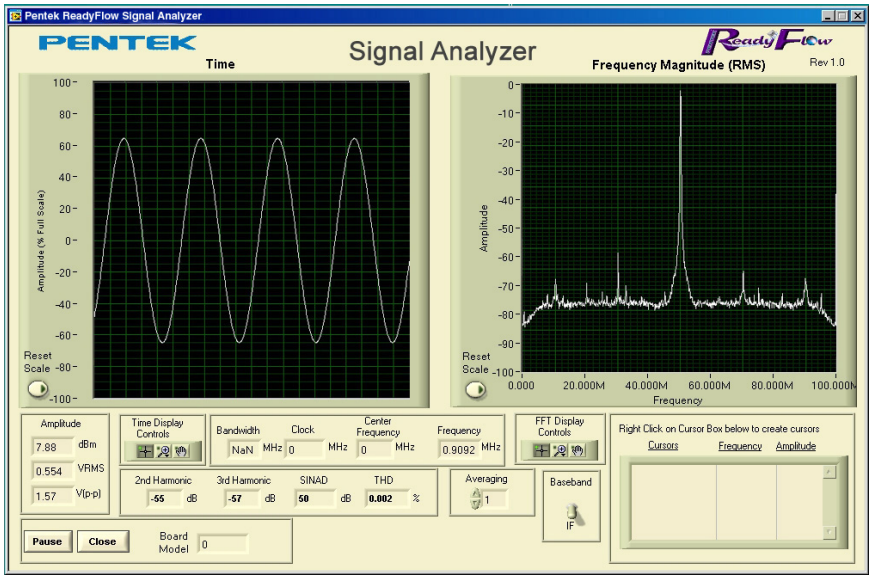
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx, Jade and Flexor analog and digital interfaces. The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek boards. A 1000-W power supply guarantees more than enough power for additional boards.

3U OpenVPX Development System for Cobalt, Onyx, Jade and Flexor Boards

Model 8267



Model 8267

SPARK Development Systems

ReadyFlow Board Support Package

Figure 70

The Model 8267 is a fully-integrated, 3U OpenVPX development system for Pentek Cobalt, Onyx, Jade and Flexor software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

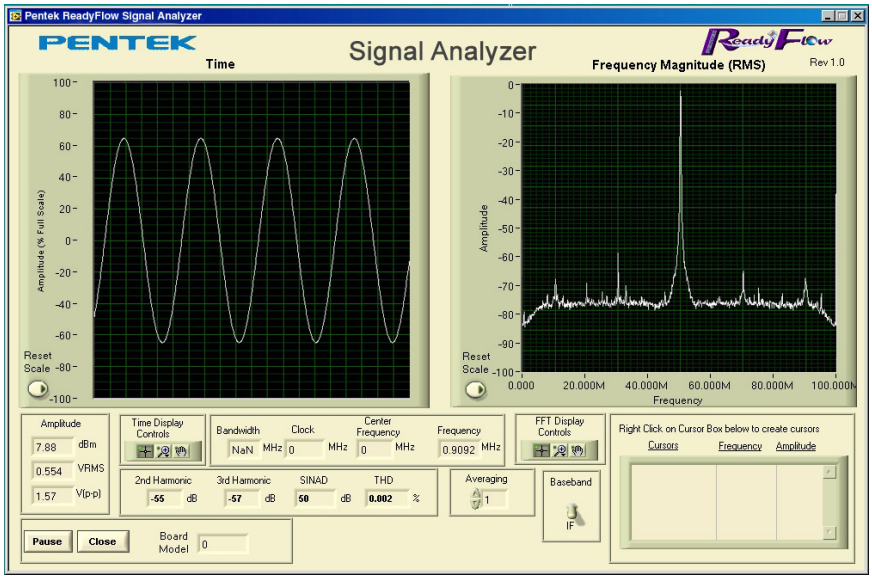
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

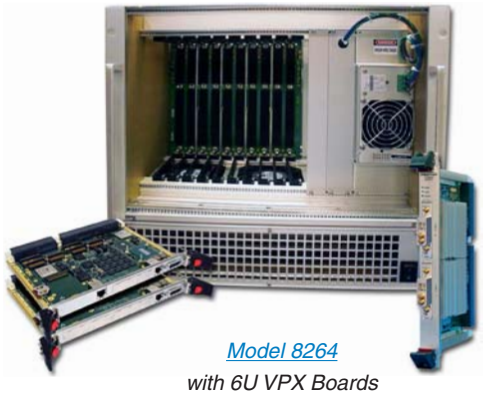
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx, Jade and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies gurantee more than adequate power for all installed boards.

6U OpenVPX Development System for Cobalt, Onyx and Jade Boards

Model 8264





Model 8264
with 6U VPX Boards

SPARK Development Systems

ReadyFlow Board Support Package

Figure 71

The Model 8264 is a fully-integrated, 6U OpenVPX development system for Pentek Cobalt, Onyx and Jade software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

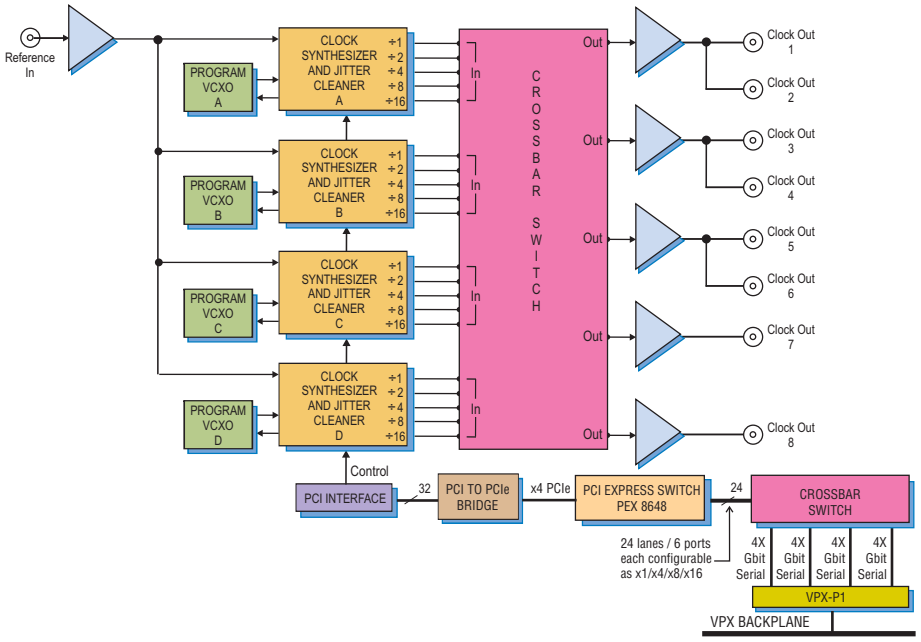
Built on a professional 6U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Jade analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19" 6U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies gurantee more than adequate power for all installed boards.

Complementary Products

Programmable Multifrequency Clock Synthesizer

Model 5391 - 3U VPX



Model 5391
3U VPX

Figure 72

Model 5391 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 5391 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 5391 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

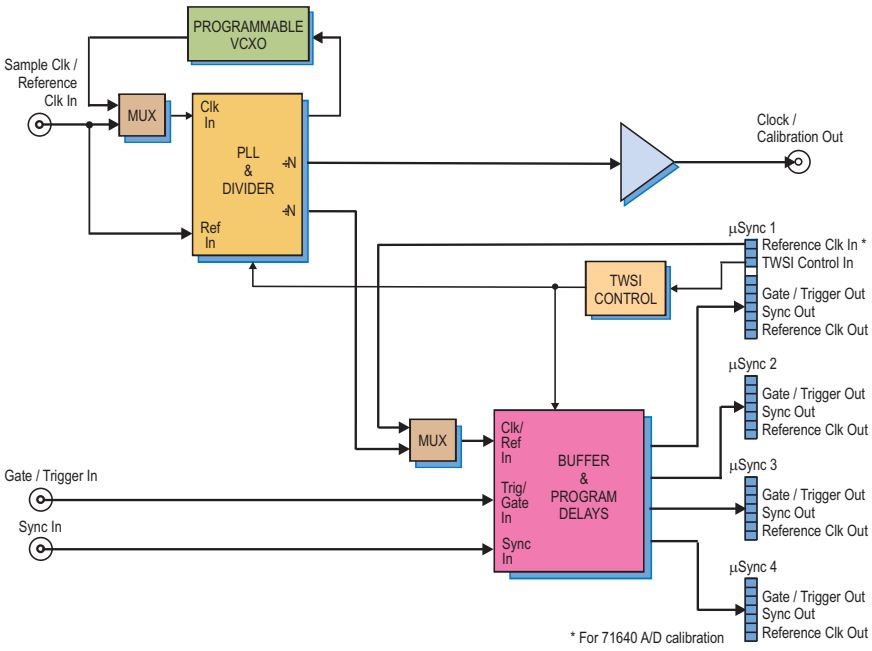
Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5391's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 5391 are also available as 6U VPX (Models 5791 and 5891 with dual density), PMC (Model 7191), PCIe board (Model 7891), AMC (Model 5691), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).

Complementary Products

High-Speed Synchronizer and Distribution Board

Model 5292 - 3U VPX



Model 5292 3U VPX
COTS and rugged

Figure 73

The Model 5292 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 5292, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 5292 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high-performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 5292 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 5292 features a calibration output specifically designed to work with the 52640 or 52740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

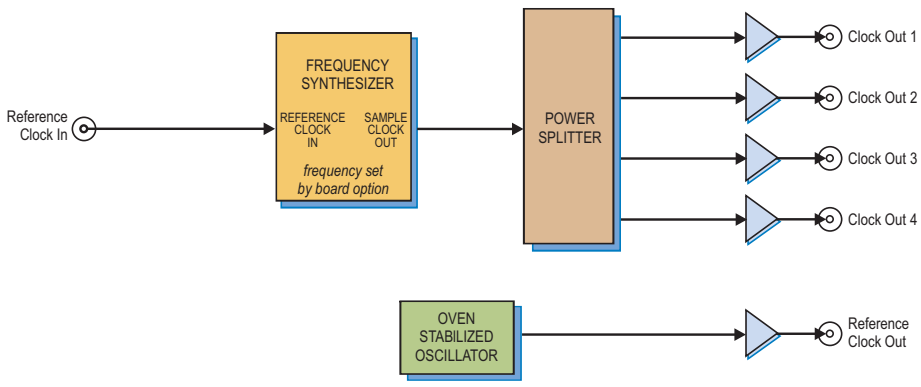
The 5292 supports all high-speed models in the Cobalt and Onyx families including the 52630/52730 1 GHz A/D and D/A 3U VPX, the 52640/52741 3.6 GHz A/D 3U VPX and the 52670/52771 Four-channel 1.25 GHz, 16-bit D/A 3U VPX.

Versions of the 5292 are also available as 6U VPX (Models 5792 and 5892 dual density), PMC/XMC (Model 7192), PCIe board (Model 7892), AMC (Model 5692), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).

Complementary Products

High-Speed Clock Generator

Model 5294 3U VPX



Model 5294 3U VPX
COTS and rugged

Figure 74

Model 5294 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx boards in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

The Model 5294 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 5294 is available with sample clock frequencies from 1.4 to 2.0 GHz.

In addition to accepting a reference clock on the front panel, the 5294 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

The 5294 is a standard 3U VPX board. The board does not require programming and the VPX P1 or P2 connector is used solely for power. The board can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Versions of the 5294 are also available as a 6U VPX (Models 5794 and 5894 with dual density), PMC/XMC (Model 7194), PCIe board (Model 7894), AMC (Model 5694), 6U cPCI (Models 7294 and 7494 dual density), and 3U cPCI (Model 7394).

High-Speed System Synchronizer Unit

Model 9192 - Rackmount

Model 9192

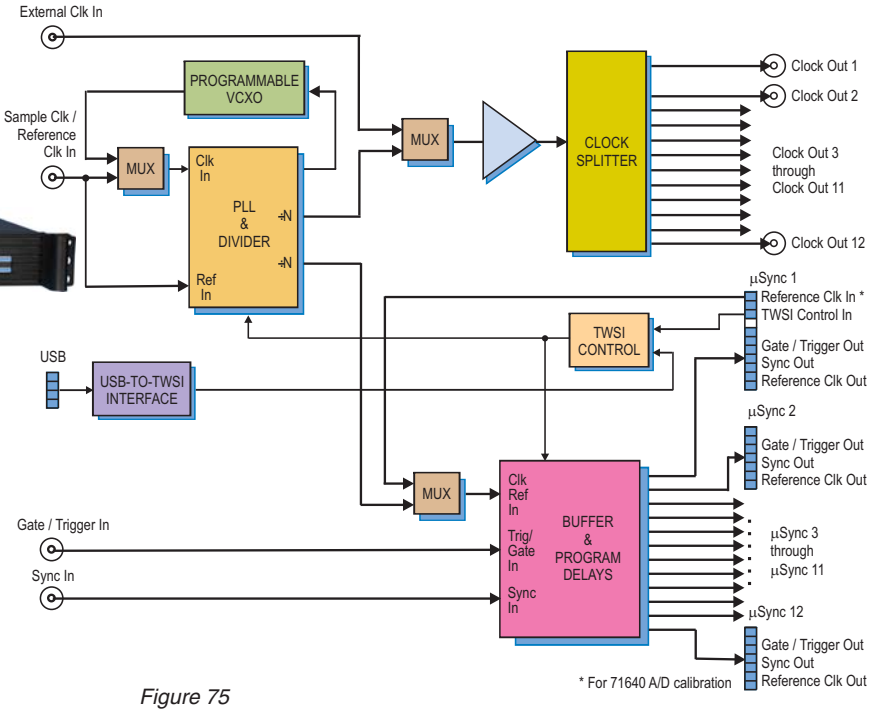


Figure 75

Model 9192 Rackmount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high-performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the xx640 or xx741 3.6 GHz A/D modules and provides a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 supports all high-speed models in the Cobalt family including the xx630 1 GHz A/D and D/A , the xx640 3.6 GHz A/D and the xx670 Four-channel 1.25 GHz, 16-bit D/A. The 9192 also supports high-speed models of the Onyx family.

Complementary Products

Talon High-Speed Recording Systems: Flexible and Deployable Solutions

High-Speed Recording Systems

Talon® High-Speed Recording Systems eliminate the time and risk associated with new technology system development. With increasing pressure in both the defense and commercial arenas to get to the market first, today's system engineers are looking for more complete off-the-shelf system offerings.

Out of the box, these systems arrive complete with a full-featured virtual operator control panel ready for immediate data recording and/or playback operation.

Because they consist of modular COTS board-level products and the flexible Pentek SystemFlow® software, they are easily scalable to larger multichannel data acquisition and recording applications requiring aggregate recording rates of up to 5.0 GB/sec or more.

Ready-to-Run Recording Systems

Depending on model, the Pentek offerings are fully integrated systems featuring a range of A/D, D/A or digital I/O resources with high-speed disk arrays.

While these systems are built on a Windows workstation and not an OpenVPX backplane, they are presented in this section because they can easily satisfy a broad spectrum of recording needs. Furthermore, users can easily install postprocessing and analysis tools to operate on the recorded data which is stored in the familiar NTFS format.

TALON RTV VALUE RECORDER

RTV Recording Systems are excellent value for under $20,000

TALON RTS COMMERCIAL RECORDER

RTS Recording Systems are designed for commercial applications

TALON RTR RUGGED RECORDER

RTR Recording Systems are designed for harsh environments

TALON RTX EXTREME RECORDER

RTX Recording Systems are designed for extreme environments

ANALOG RECORDERS

Click Here for the SYSTEM SELECTOR

DIGITAL RECORDERS

Click Here for the SYSTEM SELECTOR

Recording Systems Form Factors

Pentek's High-Speed Recording Systems are available as Lab Systems, Portable Systems, Rugged, and Extreme Systems.

RTV and RTS Lab Systems are housed in a 19-in. rack-mountable chassis in a PC server configuration. They are designed for commercial applications in a lab or office environment.

RTS Lab system

RTR Portable Systems are available in a small briefcase-sized enclosures with integral LCD display and keyboard. They, too, provide a PC server configuration and are designed for harsh environment field applications where size and weight is of paramount importance.

RTR Portable System

RTR Rugged Rackmount Systems are housed in a 19-in. rugged rack-mountable chassis. They are built to survive shock and vibration and they target operation in harsh environments and remote locations that may be unsuitable for humans.

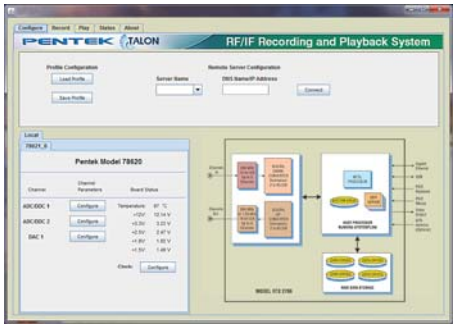
RTR Rackmount system

RTX Extreme Systems are available in a rackmount chassis designed to military specs. They are designed to operate under extreme environmental conditions using forced-air or conduction-cooling to draw heat from system components.

RTX Rackmount system

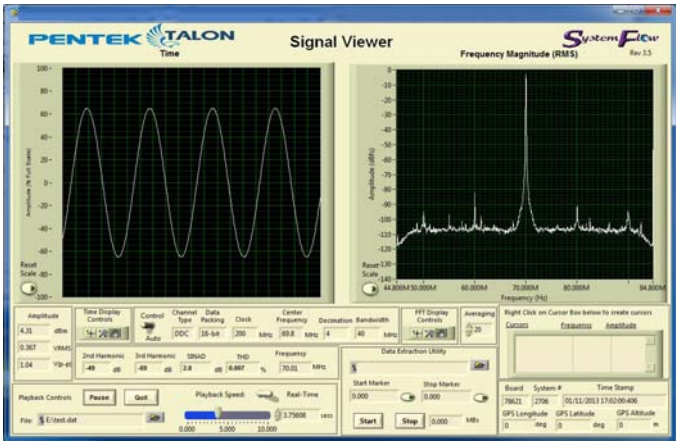
Complementary Products

Pentek SystemFlow Recording Software for Analog Recorders



Recorder Interface

Hardware Configuration



Signal Viewer

Figure 76

The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek analog high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** shows a system block diagram and includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

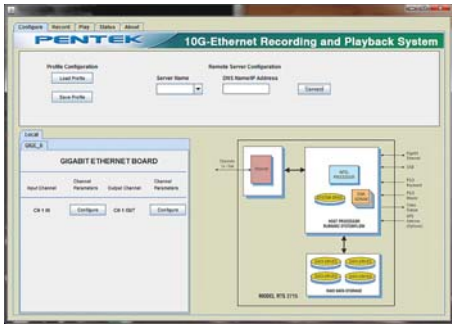
The **Hardware Configuration** screen provides a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

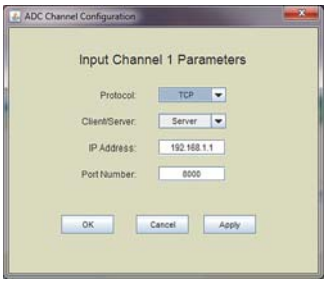
Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Complementary Products

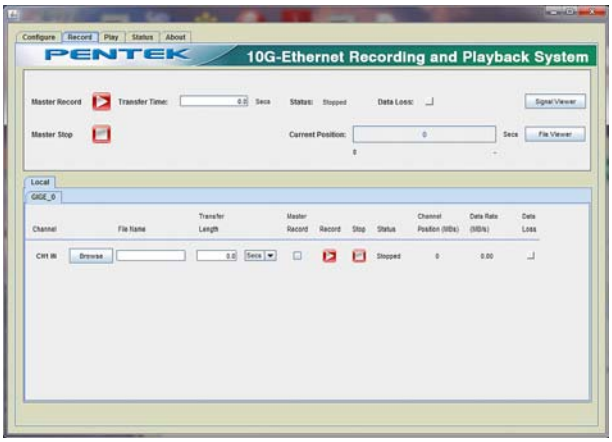
Pentek SystemFlow Recording Software for Digital Recorders



Main Interface



Hardware Configuration



Record Screen

Figure 77

The SystemFlow **Main Interface** for Digital Recorders shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream.

The **Configure** screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The **Record** screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk- full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.

Complementary Products

200 MS/sec RF/IF Rackmount Recorder

Model RTV 2601

Model RTV 2601

TALON RTV VALUE RECORDER

SystemFlow

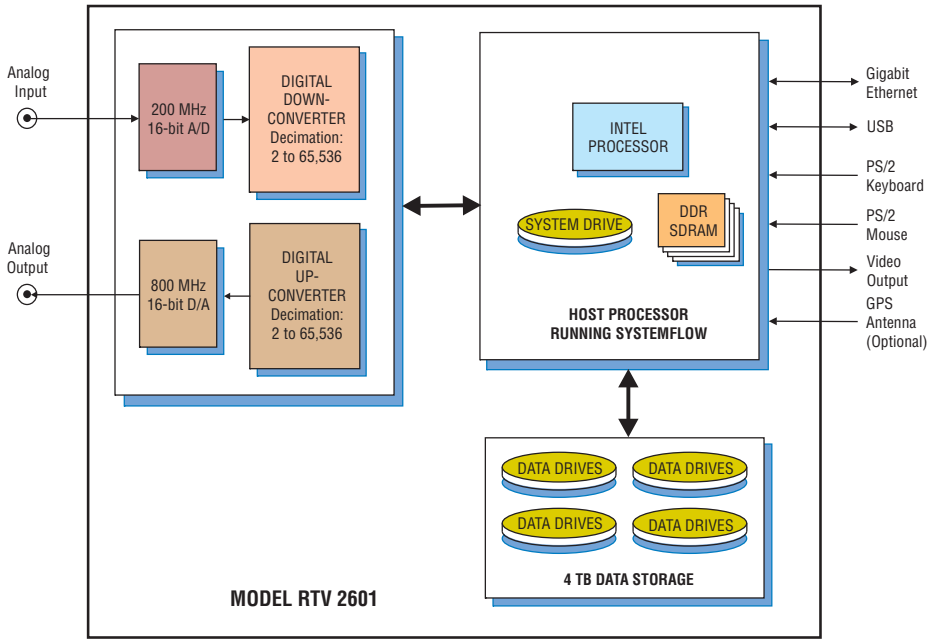


Figure 78

The Talon RTV 2601 is a turnkey multiband recording and playback system used for recording and reproducing signals with bandwidths up to 80 MHz. The RTV 2601 uses a 16-bit, 200 MHz A/D converter to provide real-time sustained recording rates to disk of up to 400 MB/sec. The A/D is complemented with a 16-bit 800 MHz D/A that provides the ability to reproduce signals captured in the field.

The RTV 2601 comes in a 4U 19 in. rackmount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available at the front. Air is pulled through the system from front to back allowing it to operate at ambient temperatures from 5 to 35 deg C.

The RTV 2601 includes a programmable digital downconverter so users can configure the system to capture signals with frequencies as low as 300 kHz and as high as 700 MHz. Corresponding signal bandwidths range from a few kilohertz to 80 MHz. A digital upconverter and D/A produce an analog output matching the recorded IF signal frequency.

The system includes a built-in sample clock synthesizer programmable to any desired frequency from 10 MHz to 200 MHz. This clock synthesizer can be locked to an external 10 MHz reference clock and has excellent phase noise characteristics. Alternately, the user can supply an external sample clock to drive the A/D and D/A converters. The RTV 2601 also supports external triggering, allowing users to trigger a recording or playback on an external signal.

The RTV 2601 includes the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder. Optionally, a GPS or IRIG receiver card can be supplied with the system for accurate time stamping of recorded data.

Complementary Products

Serial FPDP Rackmount Value Recorder

Model RTV 2602

Model RTV 2602

TALON RTV VALUE RECORDER

SystemFlow

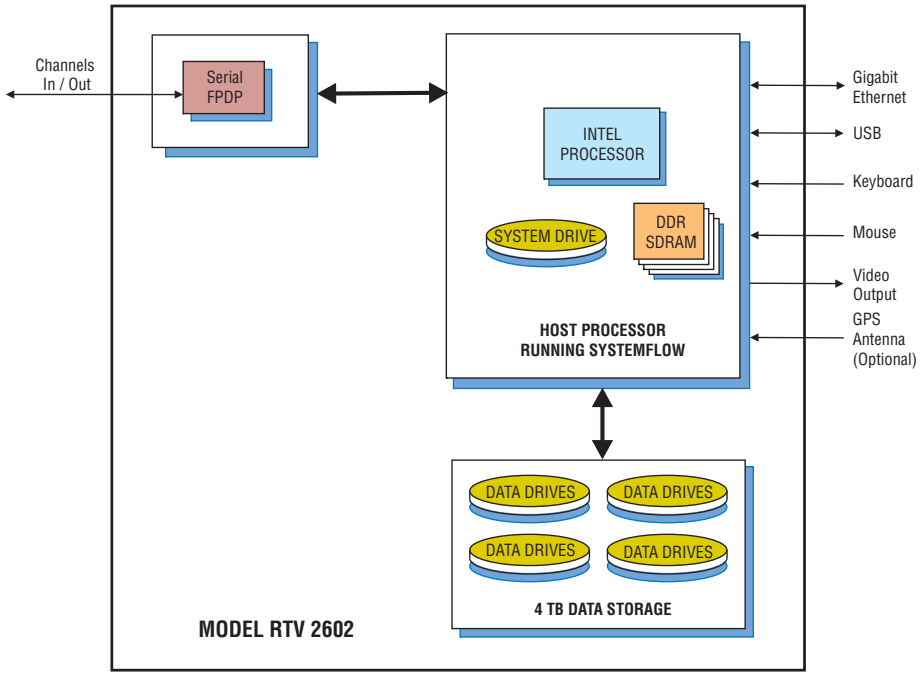


Figure 79

The Talon RTV 2602 Serial FPDP Value Recorder is designed to provide a low-cost solution to users looking to capture and play back multiple Serial FPDP streams. It can record up to four Serial FPDP channels to the built-in 4 TB RAID consisting of cost-effective, enterprise-class HDD storage. It is a complete turnkey recording system, ideal for capturing any type of streaming sources. These include live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification.

The RTV 2602 comes in a 4U 19 in. rack-mount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available in the front. Air is pulled through the system from front to back to allow operation at ambient temperatures from 5° to 35° C.

The RTV 2606 can be populated with up to four SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates. Up to four channels can be recorded simultaneously with an aggregate recording rate of up to 400 MB/sec.

Optionally, a GPS or IRIG receiver card can be supplied with the system providing accurate time stamping of recorded data. Additionally, the GPS receiver delivers GPS position information that can be recorded along with the input signals.

The RTV 2602 includes the Pentek SystemFlow recording software which features a Windows-based GUI.

Complementary Products

200 MS/sec RF/IF Rugged Portable Recorder

Model RTR 2726A

Model RTR 2726A

TALON RTS COMMERCIAL RECORDER

SystemFlow

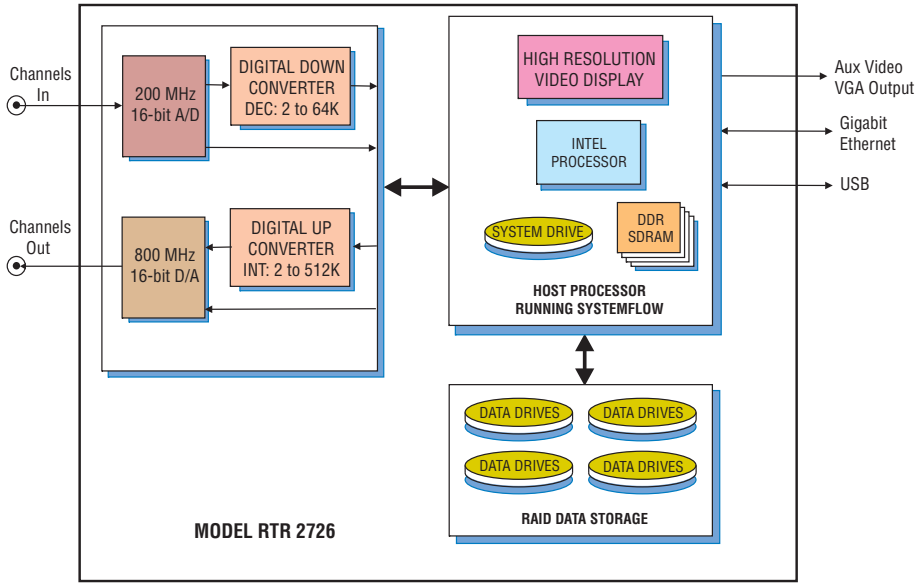


Figure 80

The Talon RTR 2726A is a turnkey, multiband recording and playback system that allows the user to record and reproduce high-bandwidth signals with lightweight, portable and rugged packages. This model provides aggregate recording rates of up to 3.2 GB/sec and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726A is supplied in a small footprint portable package measuring only 16.0" W x 6.9" D x 13.0" H and weighing just less than 30 pounds.

With measurements similar to small briefcases, this portable workstation includes Intel Core i7 processors, high-resolution 17" LCD monitors, and up to 15.3 TB of SSD storage.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, that provide fully-programmable systems capable of recording and reproducing a wide range of signals.

Included with this system is Pentek's SystemFlow recording software. Built on a Windows 7 Professional workstation with high performance Intel Core i7 processor, the system allows the user to install post-processing and analysis tools to operate on the recorded data. They record data to the native NTFS file system, providing immediate access to the data. Custom configurations can be stored as profiles and later loaded when needed, so users can select preconfigured settings with a single click.

Versions of the RTR 2726A are also available as a Rackmount Lab unit (Model RTS 2706), Rugged Rackmount (Model RTR 2746), Extreme Rackmount (Model RTX 2766).

Complementary Products

250 MS/sec RF/IF Rugged Rackmount Recorder

Model RTR 2750

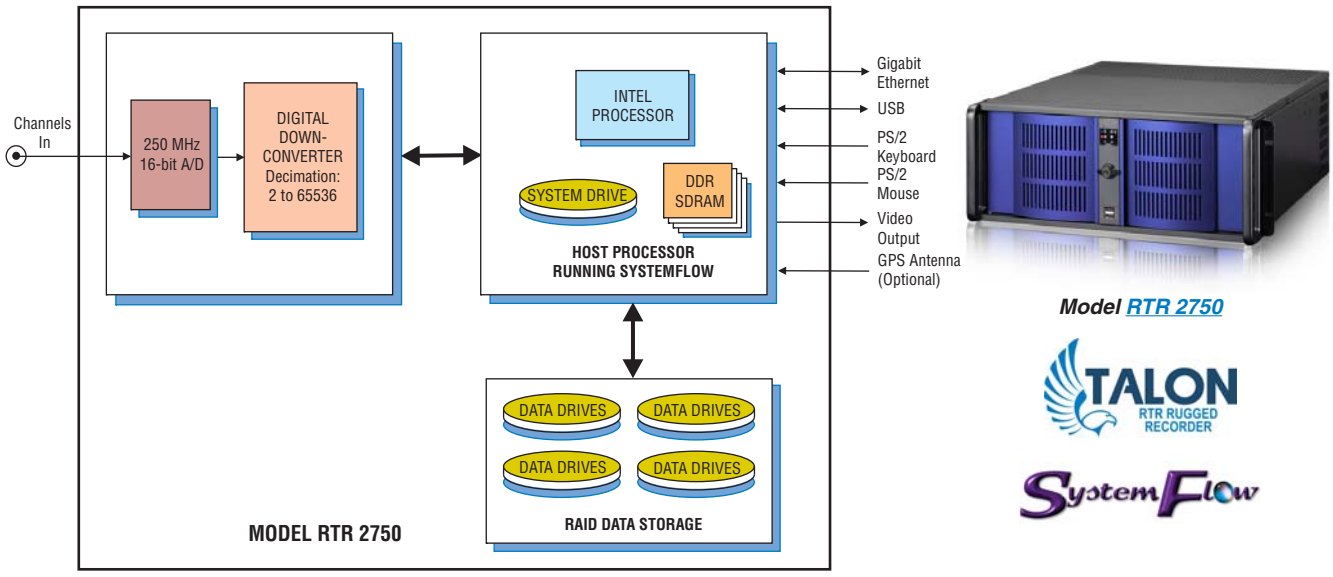


Figure 81

The Talon RTR 2750 is a turnkey recording system that provides phase-coherent recording of 16 independent input channels. Each input channel includes a 250 MHz 16-bit A/D and an FPGA-based digital down-converter with programmable decimations from 2 to 65536, thereby providing the ability to capture RF signals with bandwidths up to 100 MHz.

With options for AC- or DC-coupled input channels, RF signals up to 700 MHz in frequency can be sampled and streamed to disk in real-time at sustained aggregate recording rates up to 8 GB/sec in a 4U rackmount solution.

Designed to operate under conditions of vibration and extended operating temperatures, the RTR 2750 is ideal for military, airborne and field applications that require a rugged system. The hot-swappable solid state storage drives provide the highest level of performance under harsh conditions and allow for quick removal of mission-critical data.

A/D sampling rates, DDC decimations and trigger settings are among the selectable system parameters, providing a system that is simple to configure and operate. An optional GPS time and position stamping facility allows the user to time-stamp each acquisition as well as track the location of a system in motion.

For users who wish to create a custom user interface or to integrate the Talon recording system into a larger application, a C-callable API is also provided as part of SystemFlow. Source code and examples are supplied to allow for a quick and simple integration effort.

Data can be off-loaded through gigabit Ethernet ports or USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Complementary Products

500 MS/sec RF/IF Rackmount Lab Recorder

Model RTS 2707

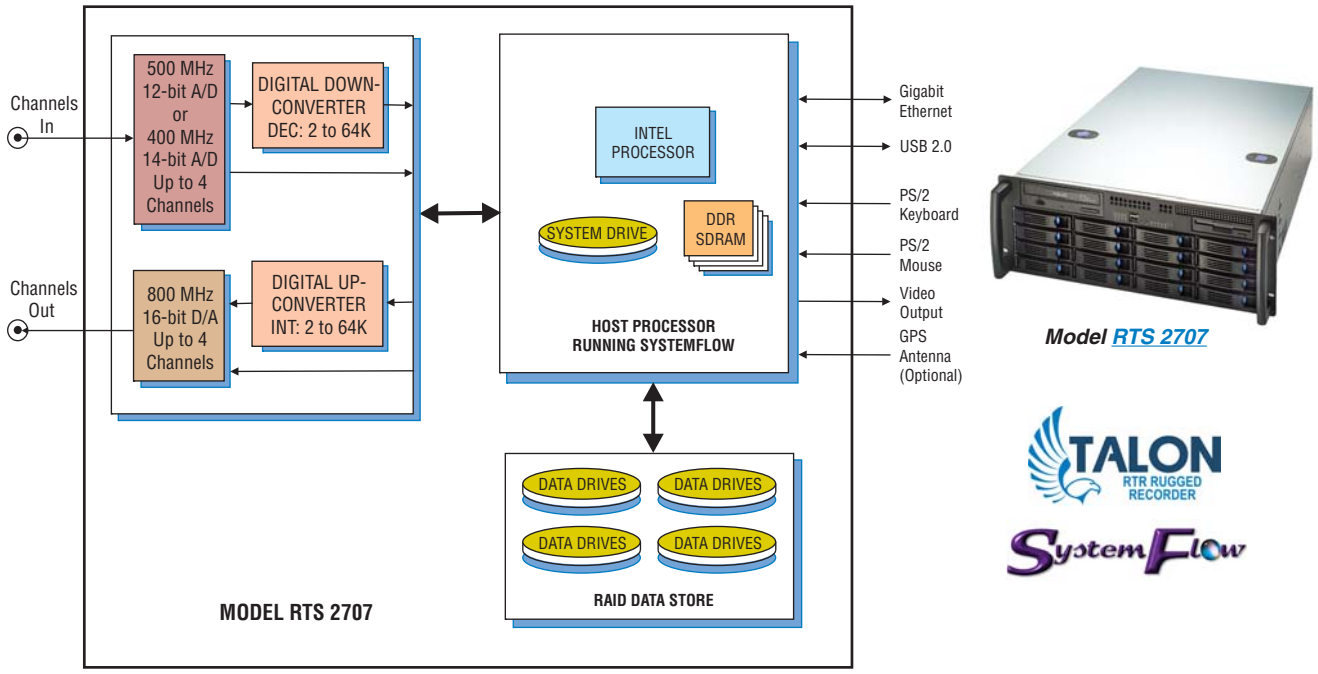


Figure 82

The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides agregate recording rates up to 1.6 GB/sec.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals. Optional GPS time and position stamping allows the user to record this critical signal information.

The RTS 2707 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder.

The RTS 2707 is configured in a 4U 19" rack-mountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

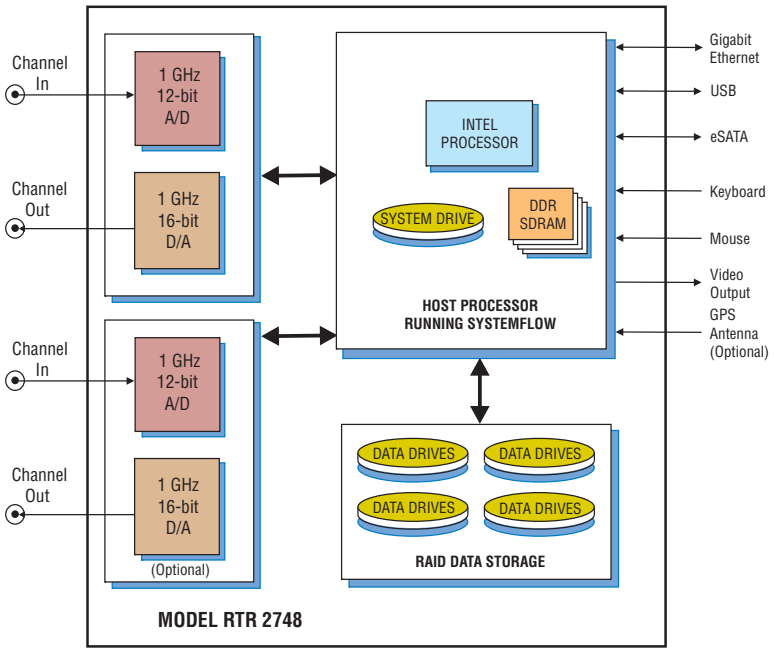
Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

Versions of the RTS 2707 are available as Rugged Portable (Model RTR 2727), Rugged Rackmount (Model RTR 2747), and Extreme Rackmount (Model RTX 2767).

Complementary Products

1 GS/sec RF/IF Rugged Rackmount Recorder

Model RTR 2748



Model RTR 2748

TALON RTR RUGGED RECORDER

SystemFlow

Figure 83

The Talon RTR 2748 is a turnkey recording and playback system that allows users to record and reproduce signals with bandwidths up to 500 MHz. The RTR 2748 can be configured as a one- or two-channel system to provide real-time aggregate recording and playback rates up to 4.0 GB/sec to an array of solid-state drives.

The RTR 2748 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converters. A built-in synchronization module is provided to allow for multi-channel phase-coherent operation. GPS time and position stamping is optionally available.

The RTR 2748 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2748 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2748 records data to the native NTFS file system that provides immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet ports, or USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2748 performs well in ground, ship-borne and airborne environments. The drives can be easily removed or exchanged during a mission to retrieve the data.

Versions of the RTR 2748 are also available as a Rugged Portable (Model RTR 2728), and Extreme Rackmount (Model RTX 2768).

3.6 GS/sec Ultra Wideband RF/IF Extreme Rackmount Recorder

Model RTX 2769

Model RTX 2769

TALON RTX EXTREME RECORDER

SystemFlow

QuickPac Compatible

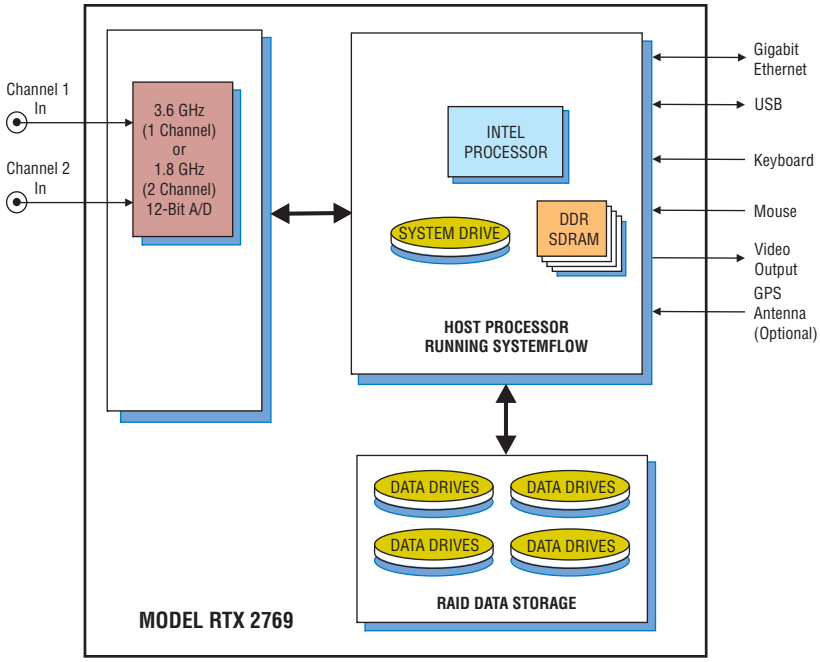


Figure 84

The Talon RTX 2769 is a turnkey system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2769 is intended for military, airborne and UAV applications requiring a rugged system.

Aimed at recording high-bandwidth signals, the RTX 2769 uses 12-bit, 3.6 GHz A/D converters. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit- or 16-bit-wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word). A high-speed RAID array provides an aggregate streaming recording rate to disk of 4.8 GB/sec.

The RTX 2769 uses Pentek's high-powered Virtex-7-based Onyx boards that provide the data streaming engine for the high-speed A/D converters. Channel and packing modes as well as gate and trigger settings are among the selectable system parameters, providing complete control over this ultra wideband recording system.

Built on a Windows 7 Professional workstation, the RTX 2769 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2769 records data to the native NTFS file system that provides immediate access to the recorded data.

The Talon RTX 2769 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the RTX 2769 are available as a Rugged Portable (Model RTR 2729A), and Rugged Rackmount (Model RTR 2749).

6 GHz RF/IF Sentinel Intelligent Signal Scanning Rackmount Recorder

Model RTS 2620

Model RTS 2620

SENTINEL

TALON RTS COMMERCIAL RECORDER

SystemFlow

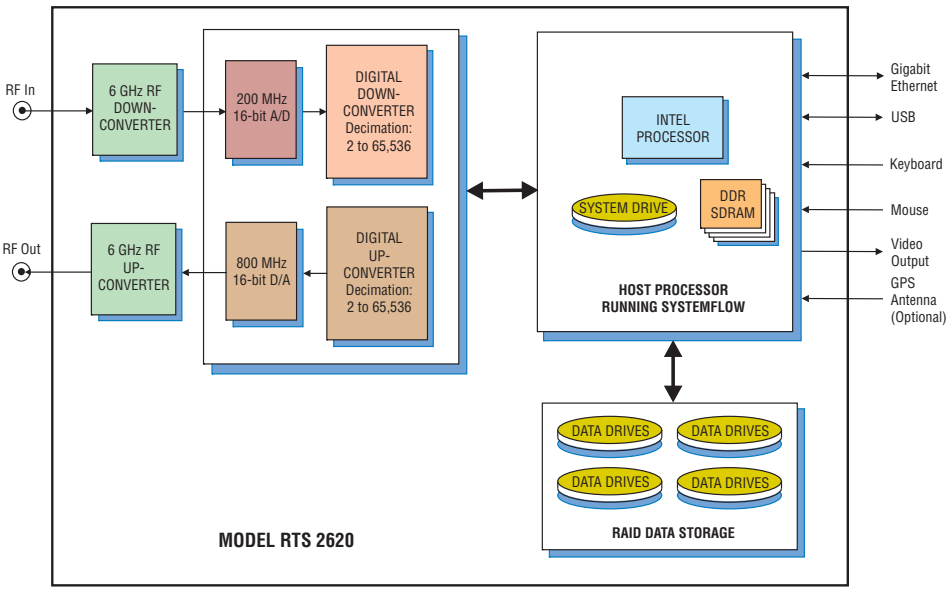


Figure 85

The Talon RTS 2620 combines the power of a Pentek Talon Recording System with those of an RF tuner and RF upconverter hardware plus Pentek's Sentinel Intelligent Signal Scanner. The RTS 2620 provides SIGINT engineers the ability to scan the 6 GHz spectrum for signals of interest and monitor or record bandwidths up to 40 MHz wide once a signal band of interest is detected.

A spectral scan facility allows the user to sweep the spectrum at 30 GHz/sec, while threshold detection allows the system to automatically lock onto and record signal bands. Scan results are displayed in a waterfall plot and can also be recorded to allow users to look back at some earlier spectral activity.

Once a signal of interest is detected, the real-time recorder can capture and store hundreds of terabytes of data to disk, allowing users to store days worth of data. The optional RF upconverter reproduces signals captured at RF frequencies up to 6 GHz.

The Pentek Model 78621 Cobalt board transceiver serves as the engine of the RTS 2620 and is coupled with a 6 GHz tuner to provide excellent dynamic range across the entire spectrum. The 200 MHz 16-bit A/D board provides 86 dB of spurious-free dynamic range and 74 dB of SNR.

The Virtex-6-based DDC with selectable decimations of up to 64 k provides exceptional processing gain while allowing users to zoom into signals of varying bandwidths. All system components are integrated into a rackmount chassis that ranges in size from 3U to 6U depending on storage requirements. Front panel removable HDDs, configured as a RAID are hot-swappable and configurable.

An optional GPS receiver and built-in PLLs allow all devices in the RF chain to be locked in phase and correlated to GPS time. GPS position information can optionally be recorded, allowing the recorder's position to be tracked while acquiring RF signals. ➤

6 GHz RF/IF Sentinel Intelligent Signal Scanning Rackmount Recorder

Model RTS 2620

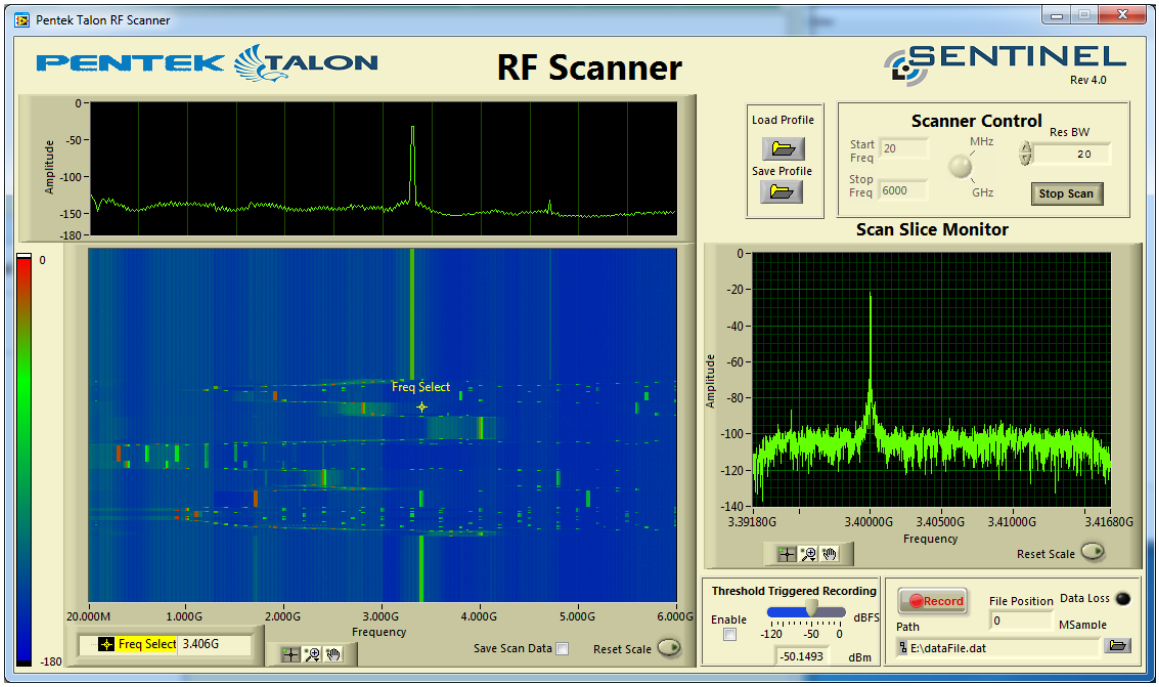


Figure 86

➤ Pentek's Sentinel™ recorders add intelligent signal monitoring and detection for Talon real-time recording systems. The intuitive GUI allows users to monitor the entire spectrum or select a region of interest, while a selectable resolution bandwidth allows the user to trade sweep rate for a finer resolution and better dynamic range. Scan settings can be saved as profiles to allow for quick setup in the field.

RF energy in each band of the scan is detected and presented in a waterfall display. Any RF band can be selected for real-time monitoring or recording. In addition to manually selecting a band for recording, a recording can be automatically started by configuring signal strength threshold levels to trigger it.

The Sentinel hardware resources are controlled through enhancements to Talon's SystemFlow software package that includes a Virtual Oscilloscope, Virtual Spectrum Analyzer and Spectrogram displays, providing a complete suite of analysis tools to complement the Sentinel hardware resources.

As shown in the figure above, an RF Scanner GUI allows complete control of the system through a single interface. Start and stop frequencies of a scan can be set by the user as well as the resolution bandwidth. All user parameters can be saved as profiles for easy setup in the field.

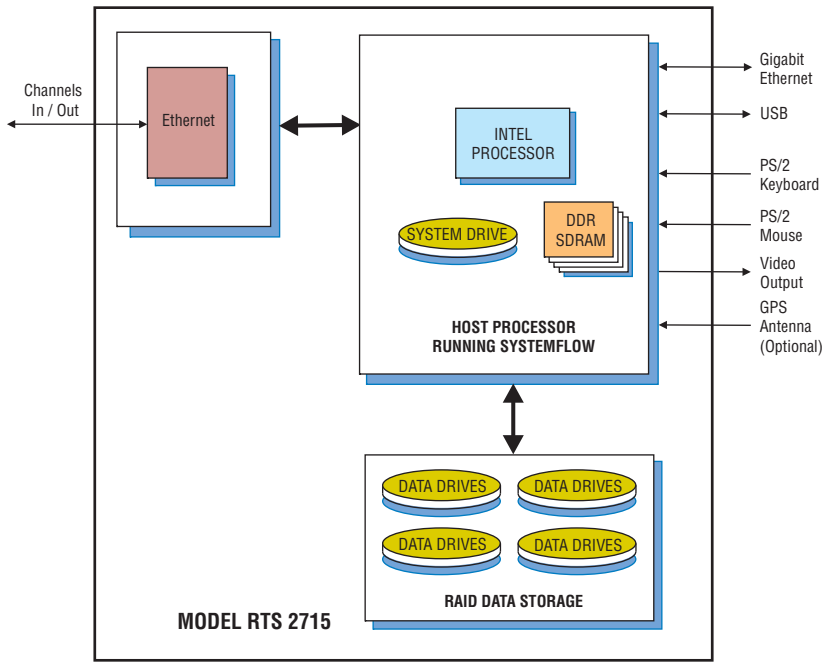
Frequency slices from the waterfall display can be selected and monitored, allowing the user to zoom into bands of interest. Threshold triggering levels can be set to record signals that exceed a specified energy. Recordings can also be manually started and stopped.

The Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded.

Complementary Products

10-Gigabit Ethernet Rackmount Recorder

Model RTS 2715



Model RTS 2715

TALON RTS COMMERCIAL RECORDER

SystemFlow

Figure 87

The Talon RTS 2715 is a turnkey rackmount lab recording system for storing one or two 10-gigabit Ethernet (10GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Versions of the RTS 2715 are also available as Rugged Rackmount (Model RTR 2755), and Extreme Rackmount (Model RTX 2775).

Complementary Products

Serial FPDP Rugged Portable Recorder

Model RTR 2736A

Model RTR 2736A

TALON RTR RUGGED RECORDER

SystemFlow

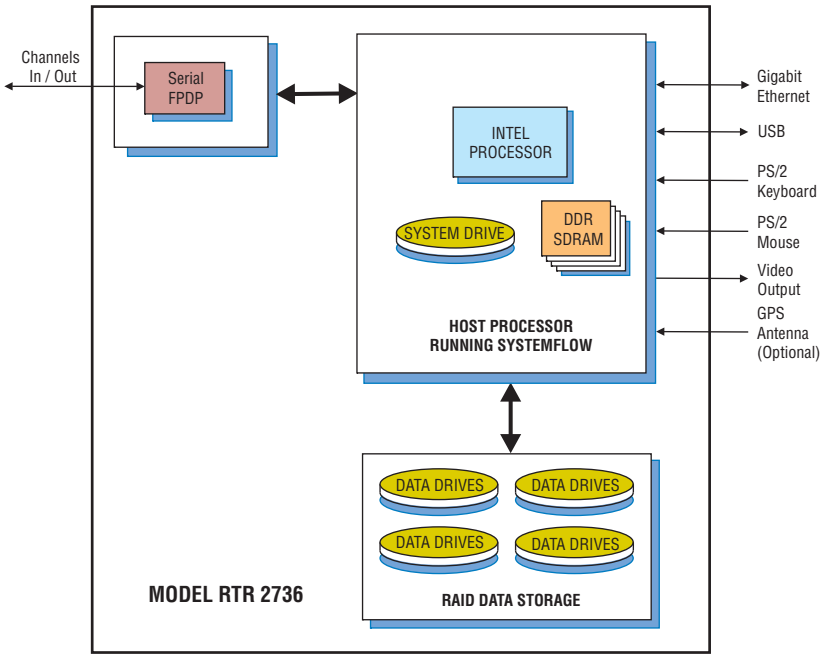


Figure 88

The Talon RTR 2736A is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, this system achieves aggregate recording rates up to 3.2 GB/sec.

The system can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per serial FPDP link.

The system includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736A is configured in portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built in extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and impact-resistant protective glass. Using vibration- and shock-resistant SSDs, the system is designed to operate reliably as a portable field system in harsh environments.

Versions of the RTR 2736A are also available as a Rackmount Lab unit (Model RTS 2716), Rugged Rackmount (Model RTR 2756), and Extreme Rackmount (Model RTX 2776).

Complementary Products

LVDS Digital I/O Extreme Rackmount Recorder

Model RTX 2778

Model RTX 2778

TALON RTX EXTREME RECORDER

SystemFlow

QuickPac Compatible

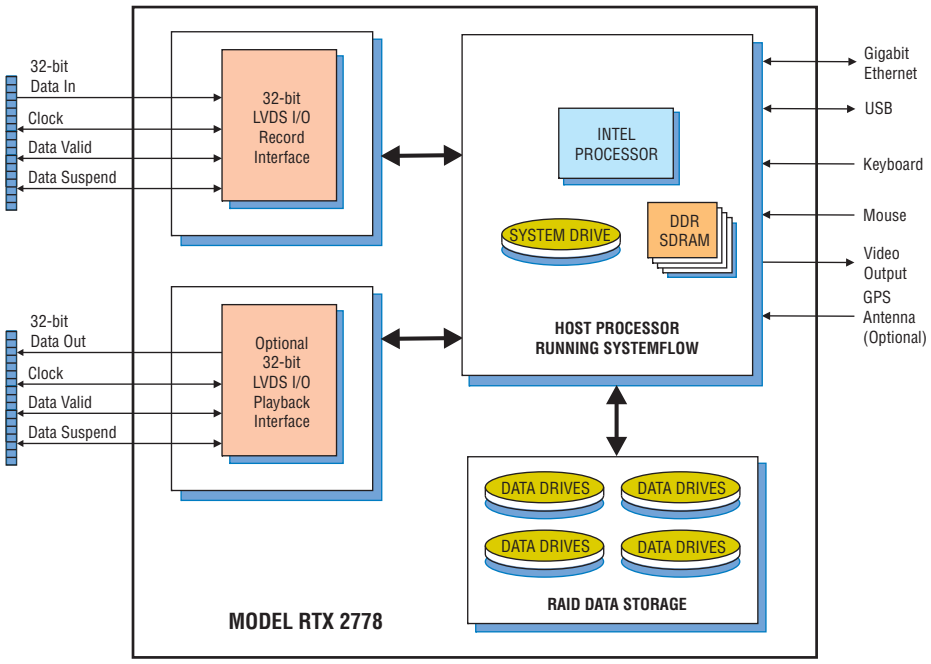


Figure 89

The Talon RTX 2778 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2778 is intended for military, airborne and UAV applications requiring a rugged system.

The RTX 2778 records and plays back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves aggregate recording rates of up to 1.0 GB/sec.

The RTX 2778 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

The RTX 2778 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Built on a Windows 7 Professional workstation, the RTX 2778 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2778 records data to the native NTFS file system, providing immediate access to the recorded data.

The Talon RTX 2778 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the RTX 2778 are also available as a Rackmount Lab unit (Model RTS 2718), Rugged Portable (Model RTR 2738), and Rugged Rackmount (Model RTR 2758).

L-Band OpenVPX Signal Processing System

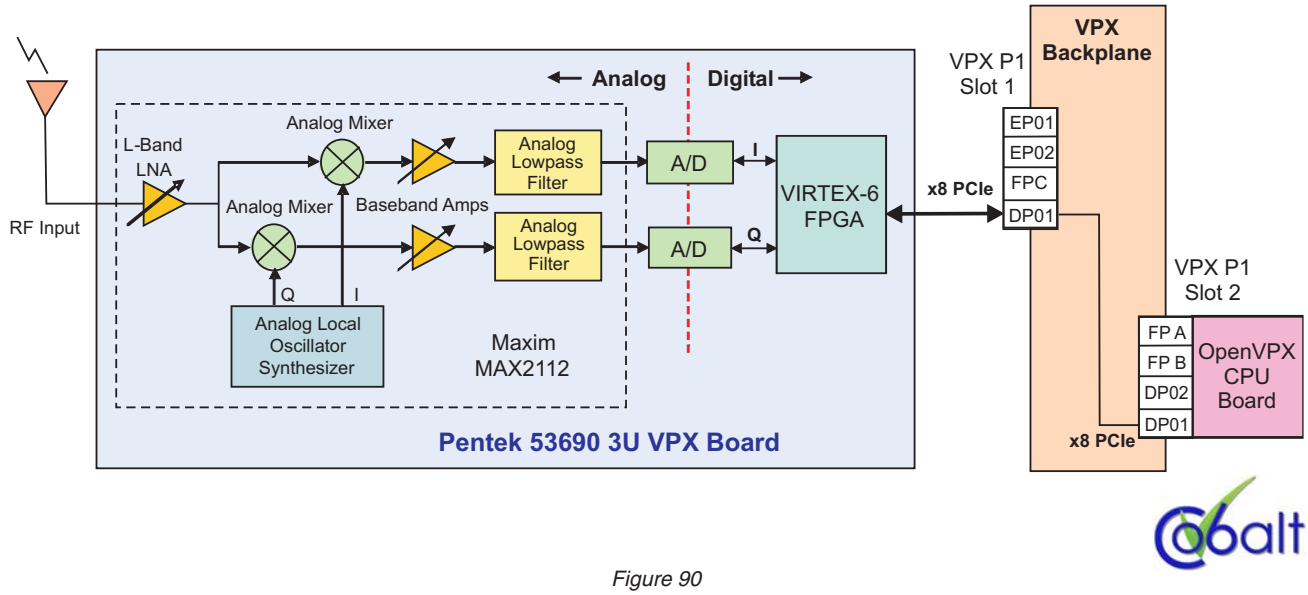


Figure 90

The Cobalt Model 53690 VPX L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 53690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz . The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size adderesses space-limited applications. Besides the Model 53690, ruggedized options are available from Pentek with the Models 71690 XMC module and the Model 57690 6U VPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.

8-Channel OpenVPX Beamforming System

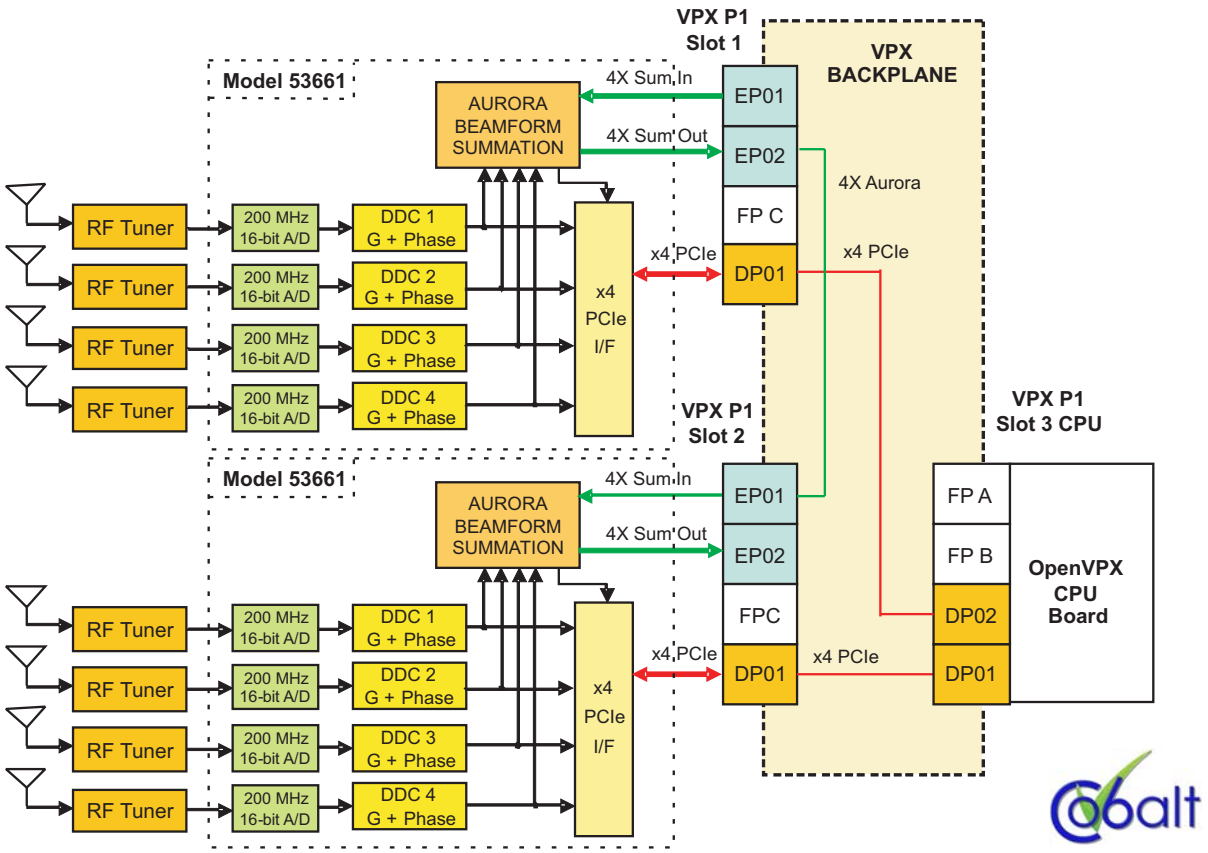


Figure 91

Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

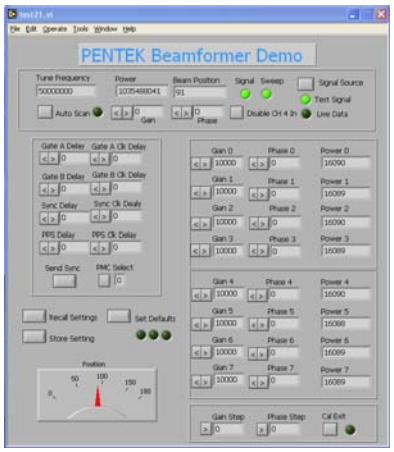
The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX "fat pipes".

The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

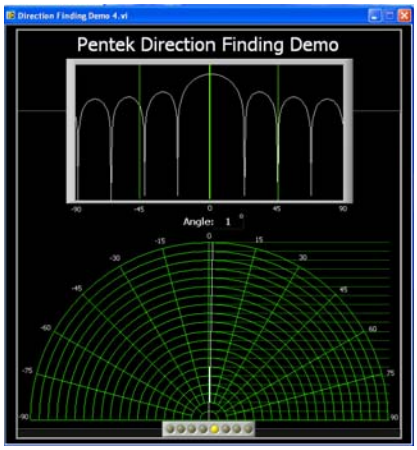
Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. ➤

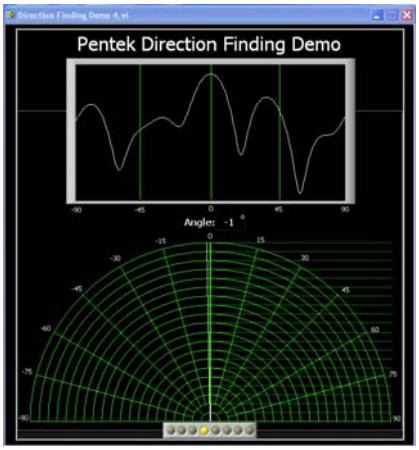
8-Channel OpenVPX Beamforming Demo system



Beamforming Demo Control Panel



Theoretical 7-lobe Beamforming Patern



Real-Life Beamforming Patern

Figure 92

➤ Beamforming Demo System

The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum sensitivity across arrival angles from -90^{O} to +90^{O} perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0^{O} angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link:
Beamforming Demo.