WHITE PAPER

Electronic warfare: an introduction to low latency COTS solutions

Fabio Ancona,
Field Applications Engineer

abaco SYSTEMS

Electronic warfare: an introduction to low latency COTS solutions

Introduction

In the conflicts of the future, dominance of the electromagnetic spectrum will be a military imperative for victory – either denying access to an enemy, or ensuring unimpeded access to friendly forces. The rate of development of sophisticated electronic warfare applications to support these objectives is, unsurprisingly, accelerating. High performance/low latency is essential in the hardware that supports such applications. COTS (commercial off-the-shelf) solutions, especially those that leverage the unique capabilities of FPGA (field-programmable gate array) technology, are now capable of delivering not only on this prerequisite – but also on other key requirements.

Low-latency processing is a key requirement for electronic warfare (EW) systems. Meeting system performance requirements and delivering EW systems that can face current and emerging threats is an ongoing battle for system designers.

The main difference between radar and EW is that an EW system must respond to a threat in nanoseconds, whereas radar can tolerate latencies measurable in milliseconds.

Threats also factor into these systems, particularly if the user is unaware of where the threat is within the EW domain. The spectrum is very broad, so requires very low latency processing because a response is required anywhere in that broad radio frequency (RF) spectrum to look for a particular threat - whereas in the radar domain, what was transmitted is known and its location understood: as such, there is some fixed latency, and a certain amount of time to respond.

Moreover, the new technologies supporting, for example, cognitive RF and cognitive EW, require a significant processing performance leap - one that must be accomplished without a significant increase in size, weight, and power.

These new methodologies rely on reconfigurable hardware and software that can detect, learn about, and adapt to new threats in the field during a mission. To enable this, the 'learn and adapt' process for the threat library becomes a feedback loop, enabling new countermeasures to be developed on the fly.

Today's aerospace and defense organizations are under increasing pressure to maintain their competitive advantage by delivering cutting edge technology faster while reducing development costs. There are three key challenges to maintaining long term tactical advantage in electronic systems:

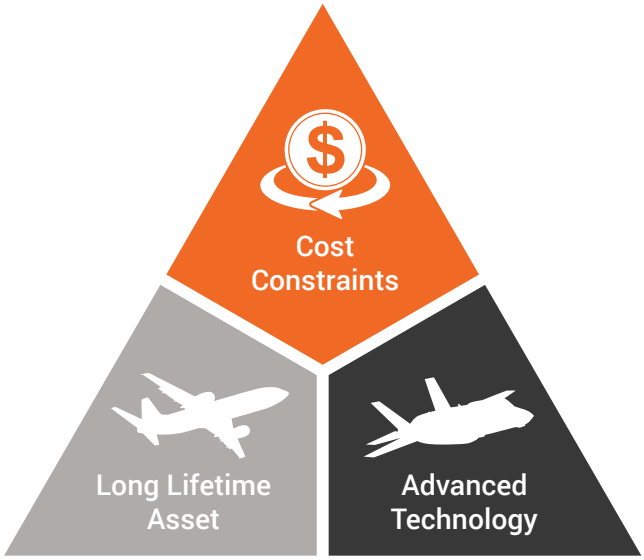

Figure 1: Three challenges for aerospace and defense organizations.

- technology challenges
- economic challenges
- system lifetime challenges

System designers constantly wrestle with the tradeoff between delivering state-of-the-art technology and the need to maintain legacy system support. From an economic viewpoint, there is growing pressure to reduce costs without sacrificing technological superiority. Building embedded computing systems with critical components that adhere to industry standard form factors and interfaces helps engineers address the three challenges of capability, cost and life cycle.

Electronic warfare: an introduction to low latency COTS solutions

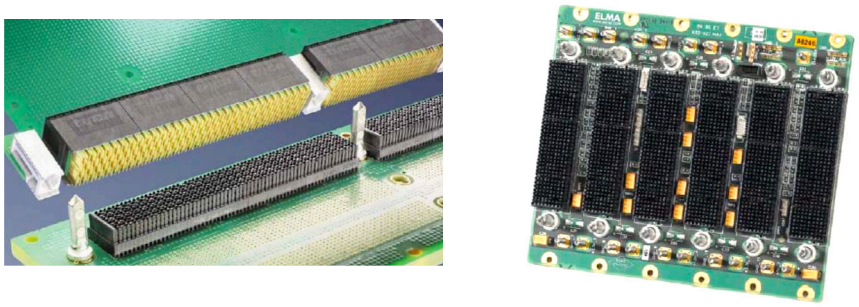

Figure 2: VPX backplane and high speed connectors.

COTS-based system design approaches tend to reduce risk and engineering cost while accelerating time to market. The concept of a platform approach to system design is that elements within a system are built on a standard interface such as FMC, PCIe®, and VPX.

There are three core benefits to a platform approach to system design:

1. There are often multiple vendors in the market; having more than one source for a technology can reduce risk should a supplier's roadmap not align with future need.

2. The ability to upgrade without re-architecting an entire system.

3. A common set of technology from the lab to deployment. With this approach, hardware and IP can be used in both the development lab and in a field deployed system with minimal changes.

The VPX standard (VITA 46) makes possible open architectures that lead to innovative new designs of high-performance embedded computing platforms. VPX systems are building on close to 40 years of VME development and are capable of delivering high performance while meeting stringent shock and vibration constraints. Rugged COTS computing applications are relying increasingly on VPX, and the standard has already been deployed extensively in data-intensive defense and military programs, particularly for applications dealing with high frequency signals.

The high-density components that enable high-speed I/O also use more power, making advanced cooling methods essential for rugged VPX designs. The Ruggedized Enhanced Design Implementation (VPX standard - VITA 48) lays out the mechanical design requirements for forced-air cooling, conduction cooling, and liquid cooling in VPX modules, providing detailed dimensions for the interface between the plug-in module and the chassis.

VPX standard and OpenVPX

VPX (also known as VITA 46) is the next generation of ruggedized compact embedded systems. After years of VME systems dominating the military/aerospace field, users have finally reached the limit of available bandwidth on the VMEbus. VPX expands the possible bandwidth, compared to the traditional VME system, by replacing the parallel bus with high speed serial buses. Much as the desktop market is transitioning from PCI to PCIe, the VME standard has been transformed to embrace the new VPX standards. The serial buses offer higher data rates while using a fraction of the routing resources. This allows the new VPX standard to focus more physical backplane resources on improving other design aspects such as supporting larger power draw and more user I/O.

The VITA 46.0-2007 standard specifies the base mechanical and electrical specifications for VPX, which maintains the 3U and 6U standard mechanical form factors that currently exist in VME and cPCI systems.

The board interconnects are high speed connectors, which allow for the use of high speed serial buses upwards of 10 Gbps and beyond.

The actual backplane connection uses either three connectors (P0-P2) for a 3U card or seven connectors (P0-P6) for the 6U card. P0 is reserved for the power and system control signals.

P1 has a handful of system control signals and the rest can be used for data bus connections between modules. Any remaining unused pins are considered user I/O and are generally routed to either the rear transition module, as additional Flash storage, or backup bus lines. All connectors, with the exception of P0, are generally routed in differential pairs.

OpenVPX is a defined set of system implementations within VPX, defining a set of system architectures and providing a framework for interoperability between modules and backplanes. With OpenVPX, system integrators can more readily architect an application-specific system based on compatible OpenVPX profiles for modules, backplanes, and development chassis. OpenVPX is poised to serve as the ideal modular format for the coming decades of embedded computing development.

Electronic warfare: an introduction to low latency COTS solutions

Designing a complete system based on OpenVPX (VITA 65)-compatible products offers advantages in terms of performance and specialized functionality. The increased flexibility provided by the standard expands the number of options to be considered, however, and requires diligent effort during the planning stages to choose the best technology and ensure compatibility between modules and backplanes.

Abaco was a founding member of the OpenVPX initiative and continues to support, across the product range, its aim of increasing interoperability between different vendors' VPX products.

FPGA Technology, Ultrascale and Ultrascale+

An FPGA is an integrated circuit (IC) that can be programmed and configured by the embedded system developer in the field after it has been manufactured. It is a semiconductor device that is not limited to any pre-defined hardware function; rather, it is highly flexible in its functionality and may be configured by the developer according to design requirements. FPGAs use pre-built logic blocks and programmable routing channels for implementing custom hardware functionality, depending upon how the developer configures these devices. They are programmed and configured using hardware description languages like Verilog and VHDL, similar to those used for an application-specific integrated circuit (ASIC).

FPGAs may be used to implement exactly the range of logical functions and features that an ASIC can implement - but in terms of flexibility of upgrading and modifying the functionality and features of FPGAs, even after the FPGA-based product has been shipped to the end-user, FPGAs really have an edge over ASIC technology.

Internal Architecture of FPGA

There are several different families of FPGAs, manufactured by semiconductor companies including Xilinx®, Altera™ and Microsemi® that are currently available on the market. These device families, when compared with one another, show slight variations in their features and architecture. Despite these, on the whole, these device families follow a common design methodology.

FPGAs comprise hundreds or thousands of logic cells. A 'logic-cell', in turn, comprises three basic components: a small lookup table (LUT), a D flip-flop and a 2-to-1 multiplexer.

As shown in Figure 3: if required, the multiplexer may be used to bypass the flip-flop. Flip-flops are binary shift registers, which are used to synchronize logic and save logical states between clock cycles. On every clock edge, a flip-flop latches a 1 or 0 value on its input and holds that value constant until the next clock edge. A LUT may be regarded as a small RAM which is capable of implementing any logic function.

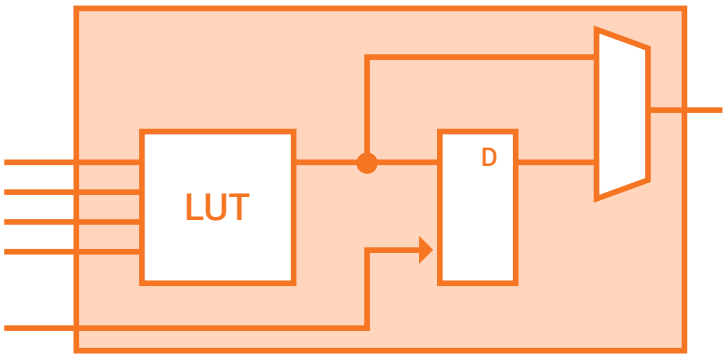

Figure 3: A basic logic cell.

Key Benefits of FPGA Technology

The global market for FPGAs is growing at an enormously high rate and the popularity of FPGAs is growing day by day. A unique feature of FPGAs is that they combine the best parts of ASICs on the one hand and processor-based systems on the other. The most compelling advantages of FPGAs are:

- high performance
- low start-up cost
- low financial risk
- cost-effective
- flexible
- short time to market
- reliable
- long-term maintenance

Xilinx's Ultrascale and Ultrascale+ families

Xilinx's new 16nm and 20nm UltraScale families are based on the first architecture to span multiple nodes from planar through FinFET (Fin field-effect transistor) technologies and beyond, while also scaling from monolithic through 3D ICs. Optimized at the system level, UltraScale+ devices deliver value far beyond a traditional process node migration – providing 2–5x greater system-level performance/watt over 28nm devices, far more systems integration and intelligence, and the highest level of security and safety. Those FPGA families include the industry's first MPSoCs (Multi-Processor System-on-Chip), which integrates the classic FPGA with a CPU.

Electronic warfare: an introduction to low latency COTS solutions

Based on the UltraScale™ architecture, the latest Virtex® UltraScale+™ devices provide the highest performance and integration capabilities, including the highest signal processing bandwidth. They also deliver the highest on-chip memory density with up to 500Mb of total on-chip integrated memory, plus up to 8GB of high bandwidth memory (HBM) integrated in-package for 460GB/s of memory bandwidth.

HBM Gen2 represents the highest DRAM bandwidth currently available.

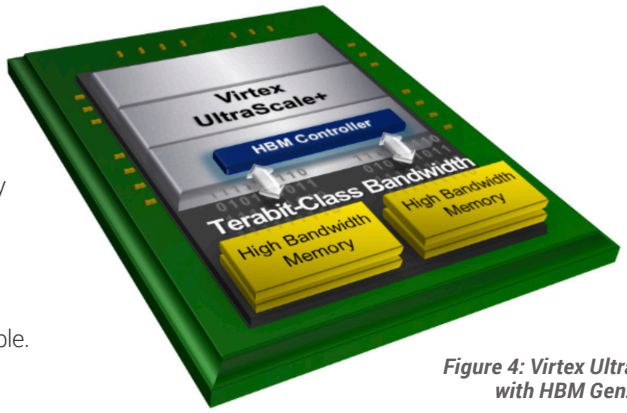

Figure 4: Virtex Ultrascale+ with HBM Gen2.

3U VPX COTS FPGA solutions for low-latency EW applications

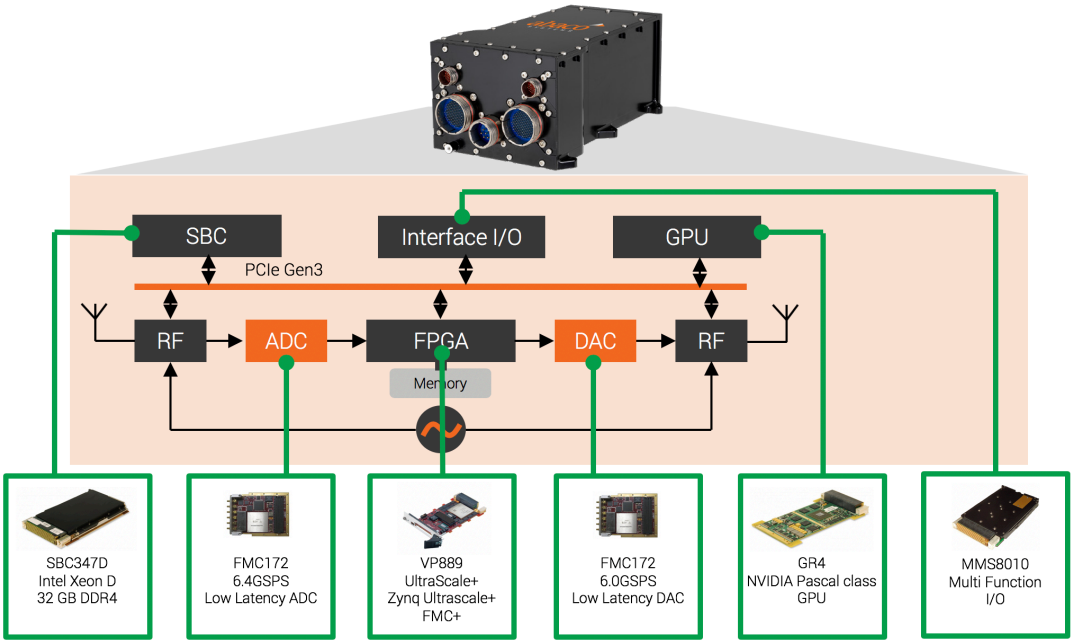

Figure 5: 3U OpenVPX Electronic Warfare System.

Performance is a critical feature in the choice of technology for low-latency applications.

Unlike digital signal processors (DSPs) and microprocessors, which execute instructions sequentially, FPGAs are capable of executing instructions in parallel and thus exceed the computing powers of DSPs and microprocessors by accomplishing more computation per clock cycle. Because of this capability of parallel processing, FPGAs can deliver many times the processing power per dollar of a DSP solution in some applications where performance and parallelism are important. Since inputs and outputs in FPGAs may be controlled at the hardware level, this helps provide faster response time and particular functionality so that the application requirements may be precisely matched.

Abaco provides an extensive range of modular, flexible and scalable system architectures based on COTS products and mixed FPGA/CPU/GPU solutions both for development and target rugged solutions.

Electronic warfare: an introduction to low latency COTS solutions

Figure 5 is an example of a COTS EW system that leverages Abaco's FMC172 FMC (FPGA Mezzanine Card) module with Wideband Low Latency I/O; the VP889 3U OpenVPX FPGA Card featuring a Virtex UltraScale+ FPGA, Zynq Ultrascale+ and FMC+ carrier board; and SBC (single board computer) and GPU (graphics processing unit) boards based on Intel® Xeon® D processors and NVIDIA® Pascal class GPUs.

It is a typical example of a 3U OpenVPX system architecture for electronic warfare applications that is flexible, modular, scalable and easily upgradable.

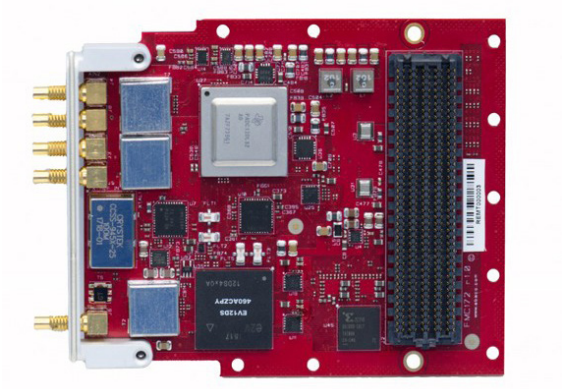

Figure 6: FMC172 – Wideband Low Latency FPGA mezzanine module.

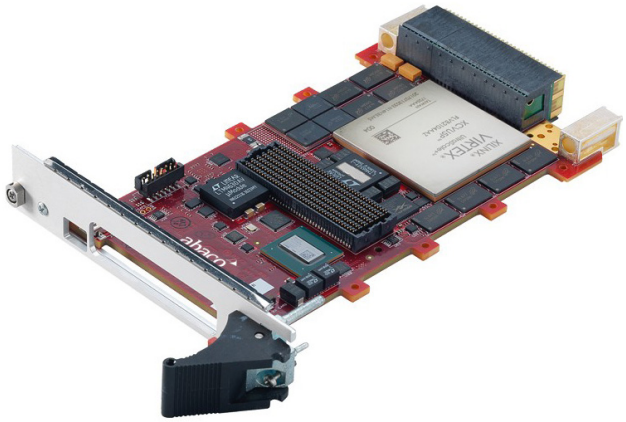

Figure 6: VP889 - Virtex UltraScale+ FPGA, Zynq Ultrascale+ and FMC+ 3U OpenVPX FPGA Card.

Conclusion

In a highly demanding market, the electronic warfare systems developer must prioritize minimal latency. However: also balanced must be the often-conflicting requirements of minimal SWaP; minimal cost (both initial purchase price and long term cost of ownership); and minimal time to deployment.

COTS products uniquely respond to all four challenges. Increasingly, FPGA technology is playing a vital role in the mix. Its flexibility and rapid prototyping capabilities deliver excellent support to the embedded system developer in greatly reducing the product development cycle to deliver the end product to the market in minimal time. The availability of COTS hardware, with different types of I/O already connected to a user-programmable FPGA device, has added great flexibility to FPGA-based system development.

Advanced COTS solutions with advantages such as flexibility, modularity, upgradability and scalability based on multi-core processors, advanced GPUs and the latest FPGA technologies such as Ultrascale+, MPSoC and RFSoC provide the optimum platform for the development of the electronic warfare solutions of the future, enabling developers to focus, not on the hardware design, but on the requirements of the application.

WE INNOVATE. WE DELIVER. YOU SUCCEED.

Americas: **866-OK-ABACO or +1-866-652-2226** Asia & Oceania: **+81-3-5544-3973**
Europe, Africa, & Middle East: **+44 (0) 1327-359444**
Locate an Abaco Systems Sales Representative visit: **abaco.com/products/sales**

abaco.com | @AbacoSys