WHITE PAPER

Selecting the Optimal DSP Solution for EW Applications

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Introduction

Invisible conflicts on the electronic battlefield are won or lost in tiny fractions of a second, with implications that can decide the success of a mission or the survival of warfighters. The conflicts are waged by embedded RF systems; some drive radar systems, while others jam and spoof radars, or jam the control signals for an IED. They may also be used to detect and locate an adversary's operations, often identifying specific types of vessels and aircraft, or to protect against detection.

Matching Technology to Specific Situations

All these EW applications are using advances in DSP technology to achieve new levels of winning capability. ADC and DAC chips now offer a broad range of sampling rates and ENOB parameters, allowing system designers to meet increasingly difficult bandwidth and SNR challenges. Their circuit density has also increased, with some individual ADC/DAC chips now supporting 8 simultaneous channels.

Application demand for more channels, more bandwidth, and lower latency is also driving advances in the processing portion of RF electronics. Not only are individual processors faster, but multiple types of processors are used, often within the same RF system. General purpose CPUs are combined with FPGAs and GPGPUs, each type inserted into a section of the processing chain that exploits its specific style of computation.

For example, radar spoofing and jamming need high compute power and deterministic throughput but not decision making or context switching, as the same math operations are performed repetitively. FPGAs, which excel at parallel throughput and determinism, are a perfect fit for the filtering and digital downconverting that are essential parts of the RF signal processing chain for these applications.

More complex sets of processors are needed to implement designs supporting cognitive EW. This new, and rapidly evolving capability relies on reconfigurable hardware and software that can detect, learn about, and adapt to new threats in the field during a mission. Cognitive EW designs begin with ADC/DAC silicon and FPGAs, then add general purpose processors, usually x86 or ARM architecture, to manage the decision making and branching that come along with cognitive techniques. Advanced designs may even include a GPGPU to apply raw processing power for some compute intensive techniques.

Current technology clearly offers RF designers a wide array of choices. To put today's options in perspective, it is useful to look at how the technology, and the choices, evolved.

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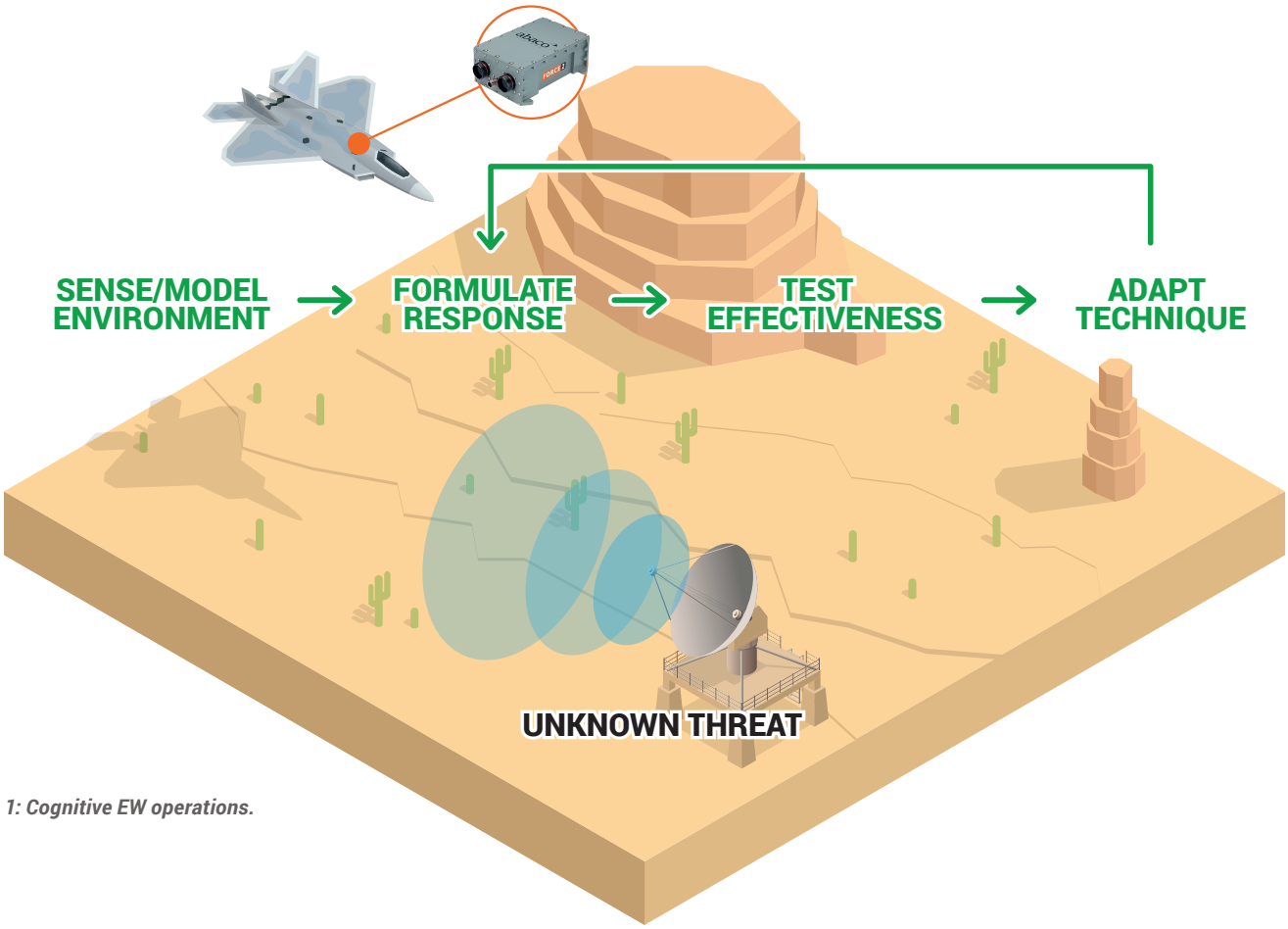

Figure 1: Cognitive EW operations.

The evolution of embedded RF solutions

Multi-board, 6U VME systems were the first COTS solutions used for RF applications. The systems were deployed in VME standard chassis and used processing and RF conversion technology from the commercial world. By basing designs on commercial electronics, these early systems were able to gain the critical advantage of rapidly advancing performance driven by the huge, non-defense marketplace. They then implemented that technology in 6U VME boards with ruggedization characteristics that made them deployable on defense platforms.

This basic approach continued to be followed across generations of RF systems and evolving defense form factors, keeping pace with expanding electronic battlefield challenges. Increasingly powerful FPGAs were employed for efficient parallel processing of data streams, while the channel bandwidth of ADC/DAC boards continued to expand. Then a leap in overall RF system throughput came when VPX backplanes replaced VME, delivering much greater system bandwidth across multiple planes of data communication.

Along with VPX, two additional technology trends enabled huge jumps in RF system capabilities. First, as mentioned earlier, advanced architectures began using different types of processors throughout the data processing chain. In these multi-architecture systems, each processor type performs a role in the chain that fits its computational strengths, with high-bandwidth data movement between processors enabled by VPX.

The second trend was increasingly powerful and more complete ADC/DAC silicon, so conversion functions that had required multiple chips were consolidated into one; the functionality of 6U ADC/DAC boards was implemented on increasingly smaller form factors, eventually fitting onto easily configured mezzanine cards, like FMCs.

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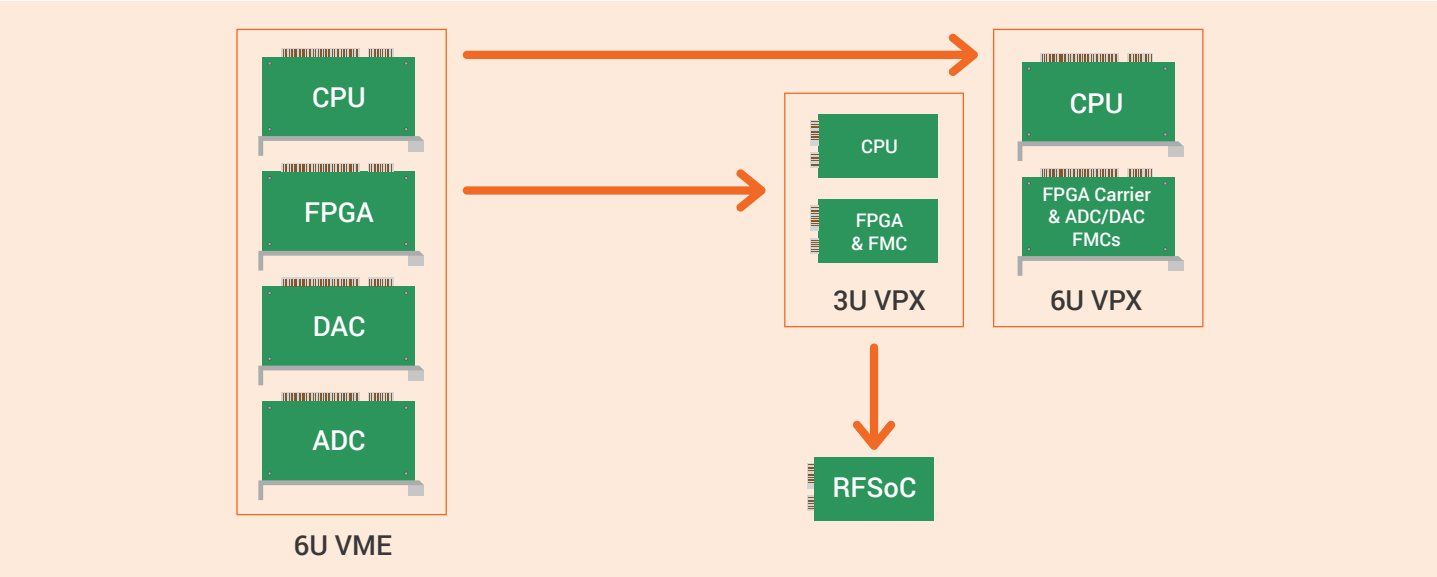

Figure 2: Evolving RF COTS solutions.

The next step was mounting the ADC/DAC FMCs on carrier cards with FPGAs, connecting the components with a low-latency LVDS data bus or the JESD204B high speed serial link. This resulted in a tightly integrated RF data acquisition and processing chain in a single slot. Even further consolidation was achieved when highly capable systems were implemented in dense processing 3U VPX systems, deployable on SWaP constrained platforms.

The broad industry trend to denser solutions has gone one step further with a recent breakthrough in processing technology, silicon that combines multiple functions on one chip, focused on a specific type of application. For RF, this is implemented in Radio Frequency System-on-Chip (RFSoC) technology that integrates ADCs, DACs, specialized logic, and multiple processing cores onto a single silicon component. Developed for commercial RF communications, RFSoC technology is also ideal for radar and EW. This tightly integrated technology is well suited to deployment in space efficient 3U VPX systems.

Introducing the VP430

A recently deployed product, the VP430 from Abaco Systems, is based on Xilinx® ZU27DR RFSoC technology. It is one of the densest analog FPGA DSP boards available, with eight ADC and eight DAC synchronized channels and featuring the ability to synchronize multiple boards for even larger system applications. In addition to the integrated ADC/DAC capability, the ZU27DR chip includes configurable FPGA logic elements, a multi-processor embedded ARM Cortex-A53 application processing unit (APU), and an ARM real time processing unit (RPU).

Integrating all of these devices onto a single chip enables the shifting of many of the analog signal processing actions - that typically take place close to the antenna in a digital receiver - into the digital domain, reducing the RF signal processing chain complexity.

With its highly integrated architecture, the VP430 packs unprecedented functionality into a single 3U VPX slot; it also reduces the backplane bandwidth load, because the bulk of the processing chain data movement is implemented within the VP430. The logic and branching capability of the integrated ARM processors means they can implement some decision and control processes, optimizing the efficiency of GPUs or CPUs in a 3U VPX system, or, for some applications, eliminating the need for an additional processors entirely. Integrating decision processing with RF signal processing makes the VP430 a complete module for implementing cognitive EW applications.

The VP430 includes the option to be built with a FireFly™ 8-channel VITA 66.4 fiber optic interface for transfers of greater than 12 Gbps for applications in which the throughput of the native VPX PCI Express® Gen3 data plane is inadequate or when a remote client requires streaming data.

As a 3U VPX module, the VP430 can be configured with a broad range of 3U VPX multi-architecture processing boards, giving system architects tremendous flexibility for new designs deploying on SWaP-constrained platforms. It also supports tech upgrades of the existing platforms with additional functionality that was not available in the past due to space constraints.

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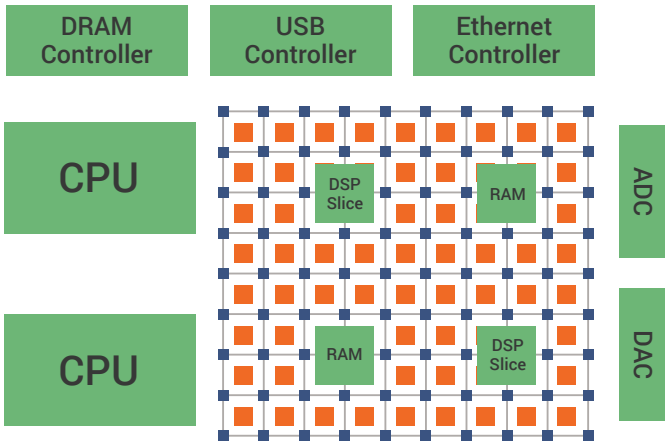

Figure 3: Functional diagram of the ZU27DR RFSoC chip.

Ideal for many applications, but not all
The VP430 offers tremendous advantages to a range of EW applications, including those that need to:

- Employ multiple, high-bandwidth RF channels for input and output
- Integrate into an existing 3U platform, or, for completely new designs, operate within a space-constrained platform.
- Reduce total system cost by consolidating multiple ADC/DAC channels to a single card.
- Reduce overall power consumption.

However, other EW applications may benefit from designs using an FPGA processing carrier card augmented by ADC/DAC FMCs; these applications include those that need to:

- Operate with only a few RF channels for input and output
- Integrate into a current system already designed around carrier-cards and simplified technology insertions and upgrades
- Decouple the processors from the ADC and ADC at the hardware level to allow independent upgrades.
- Operate in system where a single set of digital processors support multiple RF applications, each with unique analog profiles implemented using ADC/DAC FMCs
- Require extremely powerful levels of FPGA processing
- Require only modest channel count and FPGA performance, translating into very low cost solutions
- Use a processing chain that moves digitized data directly to a general purpose processor or GPGPU, without pre-processing by FPGA-based algorithms

Abaco is focused on delivering the best possible application fit
Abaco offers a comprehensive set of embedded RF solutions, including the VP430, 3U and 6U FPGA carrier boards with FMC sites, and literally dozens of ADC/DAC FMCs, spanning a huge range of channel, data rate, and signal resolution parameters. With this selection of standards-based components, system designers can focus on meeting an application's performance requirements while fitting within any legacy constraints or anticipating future upgrades.

We bring broad experience and a track record of success to embedded EW designs; our experts will engage with your solution design team to select the product mix that has the optimal application fit. With Abaco, there is no push to adopt a special design style or implement using a proprietary software tool; standard form factors and COTS components are our building blocks.

Conclusion

The challenges, and the importance, of the electronic battlefield continue to expand, driving application requirements to increasing levels of difficulty. Fortunately, embedded RF technology is keeping pace with application requirements by exploiting the performance leaps in commercial silicon, driven by the broad, worldwide electronics marketplace.

RFSoC technology is the most recent commercial RF breakthrough, offering outstanding benefits for many EW applications, especially those requiring performance across multiple channels, all within a space-constrained platform. Abaco's RF430 is the first 3U VPX COTS solution to feature the all new Xilinx ZU27DR RF system-on-chip (RFSoC) technology.

However, every application design must be approached individually, driven by requirements that include not just RF performance parameters but also form factor considerations and compatibility with legacy systems. Abaco is uniquely positioned to engage with designs teams to select an optimized embedded RF solution from a wide range of available choices, so design decisions are driven by application requirements, not dictated by technology bottlenecks.

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VP430 Details

The VP430 is a 3U VPX RF processing system featuring the transformational Xilinx® ZU27DR RF system-on-chip technology (RFSoC). The ZU27DR device used on the VP430 includes eight integrated analog-to-digital converters at 4GSPS, eight digital-to-analog converters at 6.4 GSPS, a user programmable FPGA fabric, and a multi-core Zynq ARM® processing subsystem.

The VP430 is one of the densest 3U VPX analog FPGA carrier boards available, with the ability to synchronize all 16 channels as well as multiple boards for even larger system applications. In previous generations of technology, implementing this combination would have taken four times as many boards.

Specifications:

Form factor	VPX 3U
Cooling	Air, Conduction
Conformal coating	Optional
Data rate	4000 Msps input, 6400 Msps output
Channels	8 Analog input, 8 Analog output
Operating Systems	Linus, VxWorks, Windows
Memory	8 GB DDR4
Resolution	12-bit in, 14-bit out
FPGA family	Zynq Ultrascale+ RFSoC

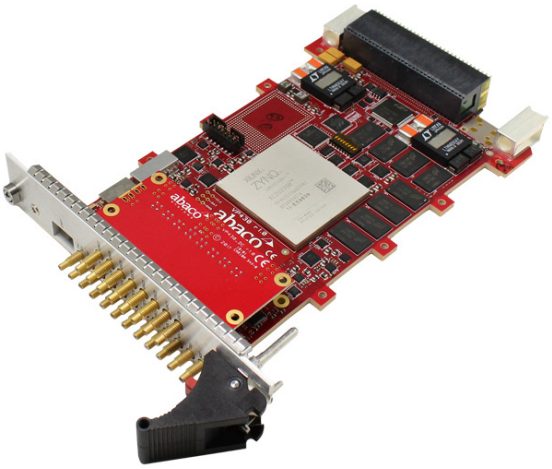

Figure 4: The VP430 3U VPX RF module.

Abaco FPGA Carrier Boards and ADC/DAC FMCs

Abaco FPGA carrier boards are built to conform with open industry standards. Combining the inherent flexibility of FPGA processing with tightly connected FMC sites, they deliver a high degree of configurability that can address a wide range of applications.

Options include the VP868 and the VP869 6U VPX FPGA boards and the VP880, VP881, and VP889 3U VPX FPGA boards. They are powered by a range of Xilinx Virtex Ultrascale+™ FPGAs and Zynq® Ultrascale+ multi-processor system-on-chip (MPSoC) silicon. The Zynq MPSoCs remove the need for a single board computer in many applications, giving designers an efficient way to maximize system performance while reducing complexity.

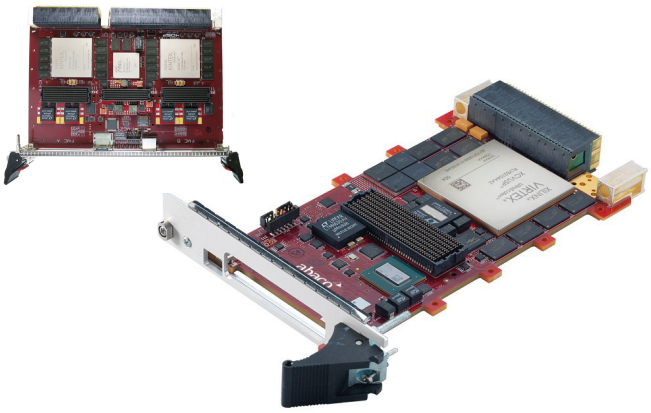

Figure 5. 6U and 3U VPX FPGA carrier boards deliver application flexibility.

Carrier board-based RF application configurations are completed with ADC/DAC FMCs; designers can select from a huge range of Abaco FMCs. These FMCs support from 1 to 8 channels, with data resolutions from 8 to 16 bits and data rates from 125 to 6400 Msps. LVDS and JESD204B interfaces are supported. These FMCs deliver modularity, flexibility, and high performance I/O to embedded EW.

Figure 6: Just a few of the dozens of ADC/DAC FMCs from Abaco Systems.

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