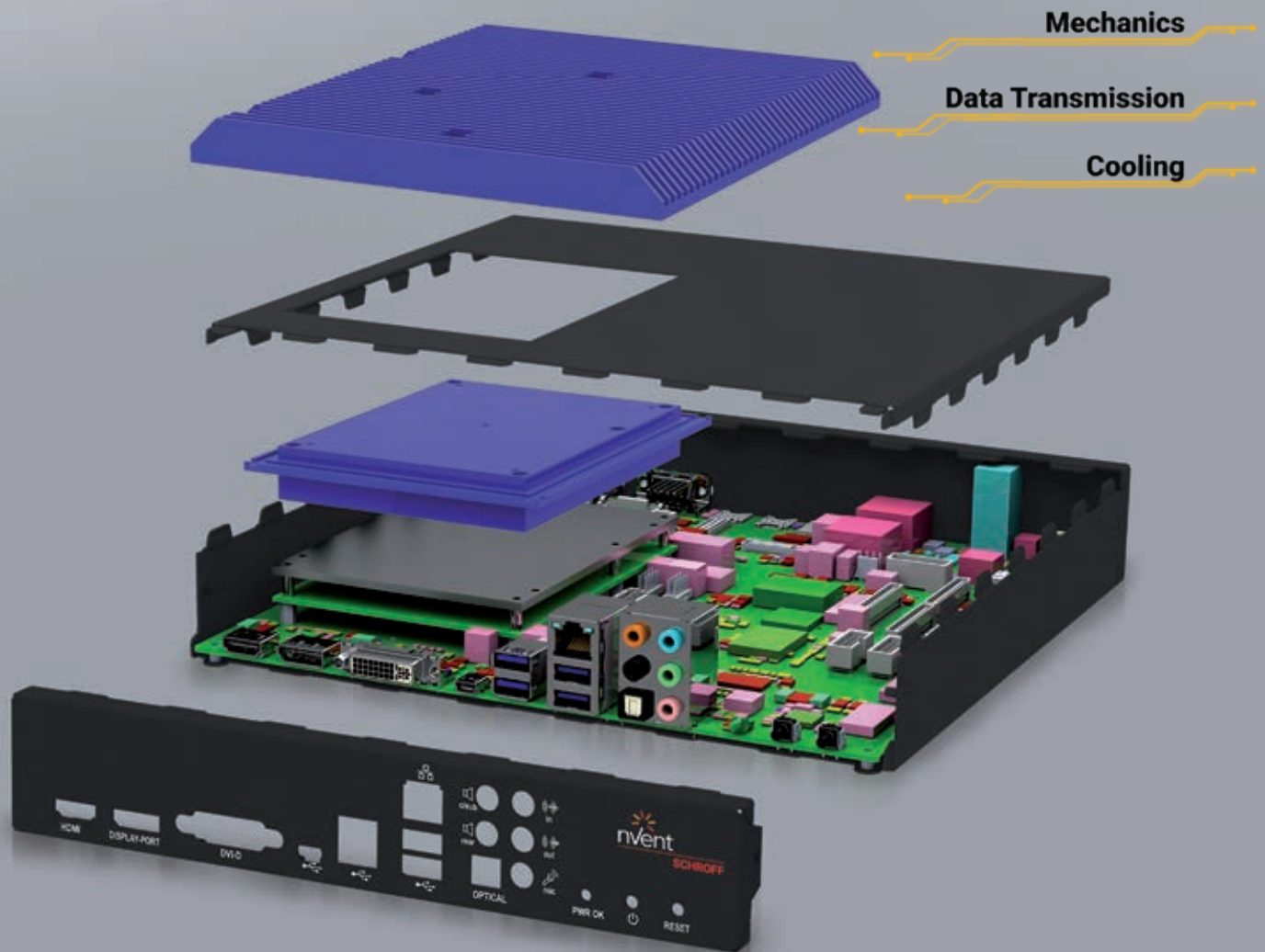




CONNECT AND PROTECT

Challenges in the development of an industrial PC based on COM

Mechanics, data transmission and cooling


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Challenges in the development of an industrial PC based on COM

MECHANICS, DATA TRANSMISSION AND COOLING

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Challenges in the development of an industrial PC based on COM

MECHANICS, DATA TRANSMISSION AND COOLING

Standards like **COM Express** exist for making customer-specific small form factor solutions. These are used to reduce the user's development time and costs. Is it possible to reduce the user's development costs even further? This white paper describes how this can be done with a modular approach to the carrier, enclosure and cooling using pre-qualified components. The white paper focuses specifically on the implementation and qualification of high-speed data interfaces and optimization of cooling through simulation and thermal measurement.

1. OVERVIEW

1.1. MARKET

The Computer-On-Module market is flourishing like never before. Tremendous growth rates are expected in the coming years, specifically due to implementation of the IIoT (the Industrial Internet of Things).

But why is computer-on-module (COM) technology so appealing to the industrial sector? Every application is different and demands dedicated electronics for recording, processing and displaying process data as a result. Production products are often unable to meet these special requirements. They might not have all the necessary interfaces, or a solution with appropriate longevity is not available, or an application might need special main board or enclosure sizes and designs that are not available on the market.

1.2. DEVELOPMENT COSTS AND TIME

If the expected production quantity for a special product is in the high thousands, ten thousands or even hundreds of thousands, it makes sense to develop a specific solution for that application from the ground up. Developing this sort of solution entails very high one-time development costs, but then the manufacturing costs of the production device are optimized for that application.

In the case of a smaller production quantity, the high development costs for a new development often blow the project out of scope and put it over budget. This makes it very useful to be able to fall back on standard components like serial-production COM modules and only invest in new development or changes for parts specific to the application.

This makes COM ideal for projects with small to medium quantities in order to reduce the initial development time as well as the development costs. Using a tested and qualified computer module and then developing only a few peripheral components from scratch—the COM carrier—also reduces the potential sources of error during development and layout. The design verification tests and qualification can focus on the newly developed or modified part of the application, making them significantly more straightforward.

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2. INTEGRATION AND FUNCTIONALITY OF THE COM CARRIER

2.1. FUNCTIONALITY

The COM module is the core of the application and the COM carrier is the interface to the application. Some key parts are needed, however, for a fully functional solution. The processor, the chipset, and the RAM on the COM module all generate heat that has to be dissipated. A cooling solution optimized for the application is necessary for this reason. Sensitive electronics need to be protected by an enclosure designed to protect against physical contact, dust, water, vibrations or other environmental factors. The heat generated by the electronics is dissipated to the surroundings by the enclosure.

The user also has the option of developing their own enclosure solution matched specifically to the application. During development, the user has to find a solution for EMC protection, IP leak protection and heat dissipation. Falling back on existing enclosure solutions that have already been tested for EMC and IP protection is the simpler option here as well. This is also true of the cooling. The enclosure typically has to be adapted to the application. Factors such as the size, number and position of cut-outs for interfaces and dimensions of heat sinks are among the key aspects to consider. Configured enclosure models, such as the Schroff Interscale Chassis, simplify this task substantially.



Figure 1: Small form factor system based on COM Express

2.2. INTEGRATION

Additional aspects have to be considered for the mechanical systems. This includes, for example, how and where the enclosure is to be mounted. This sort of small form factor solution is frequently mounted on walls, mounting plates or various points in a machine. Options for installation include horizontal rail installation or installation on a monitor using a VESA adapter. In some cases, an electrical cabinet will have the assembly space to install the system using a 19" mounting bracket. Support for the desired type of installation or the presence of the corresponding mounting adapter on the enclosure should be taken into account when selecting the housing.

Integration represents a key cost factor when setting up a small form factor system. This is typically performed by qualified personnel. Every minute that can be saved means a significant cost reduction. The fewer fasteners the enclosure needs, the shorter the integration time. The easier the assembly, the faster integration can be accomplished. A reduction in integration time becomes especially appealing in the case of large quantities because the reduced costs multiply with the number of units.

3. SIGNAL INTEGRITY IN COM CARRIER DESIGN

3.1. CHALLENGE THROUGH INNOVATION

Compared to current requirements, it was significantly easier in the past to develop and verify a COM carrier or an electronic design in general. In the times of PCI, PCIe Gen1, SATA 150 or USB 2.0 and similar slow data rates, the requirements for the design of the transmission path, materials in use, components and power integrity were very moderate. Even the effects of production tolerances and interference factors along the transmission paths were usually negligible or, at least, could be tolerated in large ranges. Due to ever-increasing data rates, the situation is changing and a few aspects have to be taken into account as early as the development stage. This is leading to many new challenges and critical points. The following sections examine these points in the development and verification of a COM carrier in greater detail.

Before starting development on a COM carrier, some information needs to be known about the SI/PI features (Signal/Power Integrity) of the components to be used and bus types to be routed. You have to know exactly which parameters have to be maintained and considered critical for each bus system, which requirements are to be met and how they can be achieved with the smallest possible cost expenditure for the design.



Figure 2: COM-carrier

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3.2. CHARACTERISTIC IMPEDANCE

One of these requirements is likely the most well-known: Characteristic impedance. This is defined, for example, between 70 ohms and 100 ohms for PCIe Gen 3 signal traces. The following diagrams show that the impedance value is not the sole decisive factor. Here are simulated values from transmission paths in three different designs with the same impedance around 85 ohms and an overall length of about 180 mm.

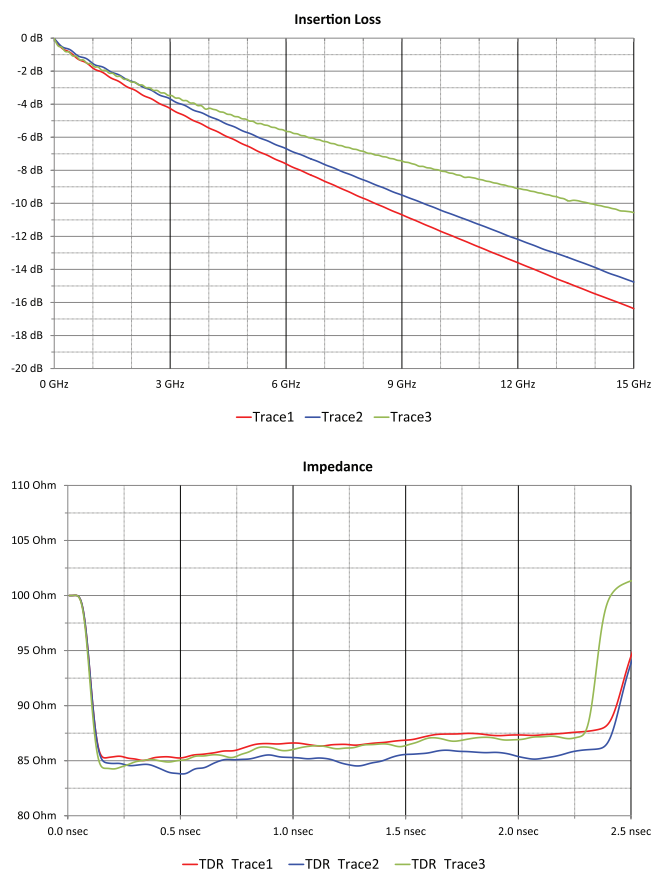


Figure 3: Insertion loss and impedance

Although all of the lines here have the same length and a differential impedance of about 85 ohms, a substantial difference is apparent in the losses in frequency domain. Accordingly, the voltage levels (eye pattern) of the signal at the receiver differ significantly.

This example is intended to show that impedance is just one parameter of many and that the transmission behavior on the path is made up of a combination of various parameters. The transmission properties can be improved significantly by using better components, materials or additional printed circuit board layers. But this increases the costs and can ultimately make the

product uncompetitive. By optimizing PCB design, you can avoid the use of low-loss material in a COM carrier, allowing more flexibility in PCB procurement and a reduction in material costs.

3.3. OPTIMIZATION THROUGH SIMULATION TOOLS

The use of simulation tools accompanying development is a necessity in order to optimize the PCB design without having to contend with any technical risks. We began optimizing the designs of our high-speed backplanes with the help of simulation programs more than a decade ago. This approach makes it possible to improve the transmission quality of the PCB design significantly while simultaneously lowering the material costs and development time. Development without using simulation tools is no longer feasible at the data rates of 40 Gbps and 100 Gbps that are typical of transmission on backplanes today. Using simulation tools when developing a COM carrier is also a necessity.

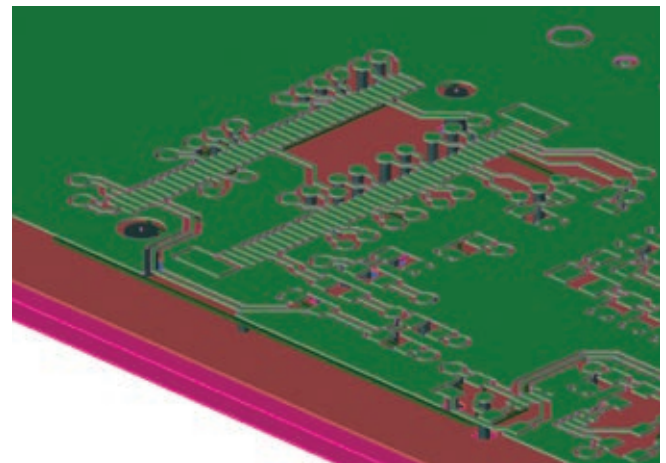


Figure 4: Fanout on M.2 connector (outer layers)

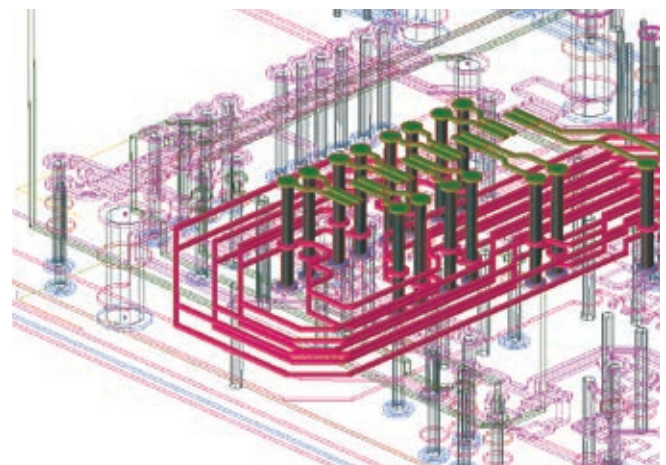


Figure 5: Fanout on M.2 connector (inner layers)

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A frequent occurrence is a situation where the position of the input/output connectors is predefined on the carrier due to mechanical requirements that cannot be changed. This means that signal and power routing has to be adapted to these requirements. This is where expertise and years of experience in backplane development plays a role in helping to define the optimal path for signal lines and power planes and use of PCB materials. If necessary, pre-layout simulations should be run to get some initial impressions regarding the feasibility and any potential problems. After the routing tests have been done and an initial carrier PCB layout is available, the critical areas of the layout should be simulated using a 3D EM simulation tool and the carrier layout is optimized based on the results.

The following example demonstrates the utility of such optimizations. In this case, the 4x PCIe Gen3 transmission path has been optimized for an M.2 connector. The images show a cutout of the COM carrier layout at the M.2 connector after the initial rough draft.

3.4. FUNCTION OF SIMULATION TOOLS

This carrier layout was then simulated and its parameters were combined into the complete PCIe transmission path (from transmitter to receiver) together with the typical parts of the transmission channel. The red curve on the bottom in the graph shows the losses in the frequency range over the entire transmission path in the first draft of the carrier layout. Through simulations and subsequent optimizations of the fanouts and trace arrangement in the layout, it was possible to create a noticeable reduction in losses in the final version of the carrier. The blue line on the graph shows the losses for the overall path (from transmitter to receiver) in the final carrier design.

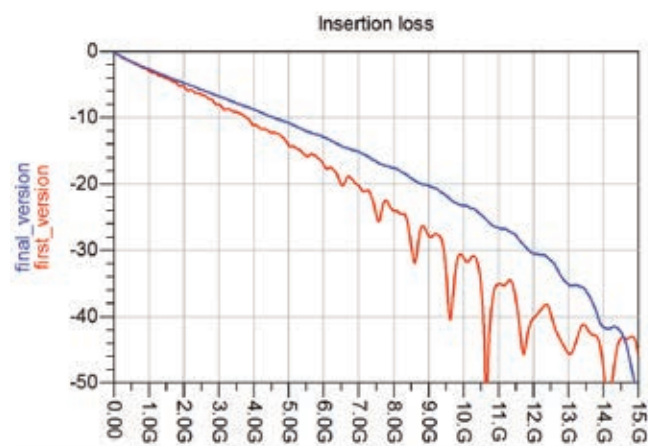


Figure 6: Insertion loss

Accordingly, this also significantly improved the eye pattern of the signal at the receiver. In this case, the simulated transmission path had had a sufficient eye pattern opening for PCIe Gen3 but hardly any clearance relative to the prescribed limit values, creating the real risk of exceeding limit values due to component, production or material tolerances.

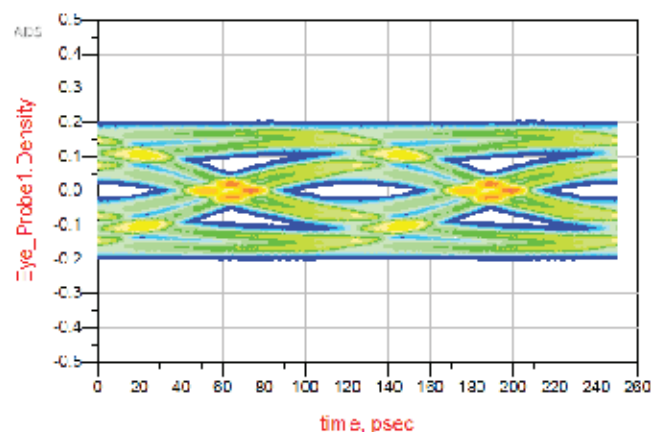


Figure 7: PCIe eye pattern before optimization

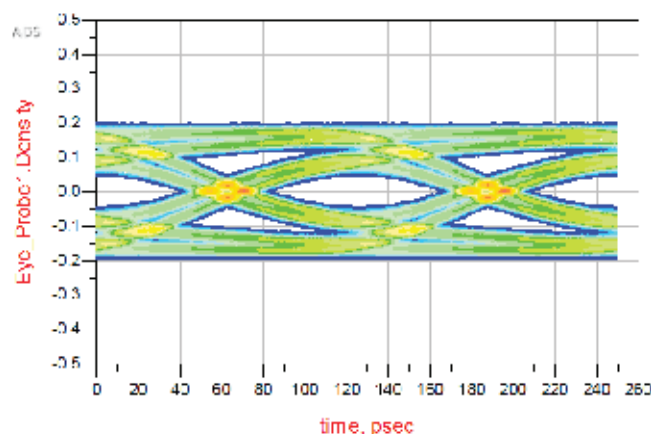


Figure 8: PCIe eye pattern after optimization

3.5. OPPORTUNITIES AND RISKS IN OPTIMIZATION

When carrying out these kinds of optimizations, it is important to know which modifications in the layout lead to which changes in the overall design. It is entirely possible, for example, for certain parameters to be improved while deteriorating the characteristics of other transmission paths. The complete layout has to be viewed as a coherent system and the mutual influences of parameters have to be taken into account as well.

Challenges in the development of an industrial PC based on COM

State-of-the-art serial bus systems have data rates in tens of Gbps per differential pair and have very short bit periods as a result, meaning that several bits can be on one data line in a COM carrier simultaneously. The voltage level of signals and the signal-to-noise ratio are also very low in current serial bus systems. This all makes them prone to interference. If the transmission path is not designed optimally, reflections, multiple reflections, jitter, mode conversions and similar effects can arise quickly, distorting the signal, increasing the bit error rate (BER) and, ultimately, lowering the data throughput. In addition, some COM carriers have active components such as PCIe switches or FPGAs, that have to be supplied with power. Even the design of the power traces and planes to these fast-switching active components has to be made carefully so that the power reaches the load with as little loss as possible. Since the power consumption of these components can change abruptly, fast changes in current draw have to be expected. This means the power consumption and, as a result, the current profile have high-frequency portions that have to be routed to the load to remain as complete as possible. In other words, the power traces and power planes on the carrier PCB have to be treated as a power transmission path with an impedance that has to be carefully controlled. Here it depends how the lines or power planes are defined and routed, which voltage sources are used, how filtering and coupling are implemented and where the components are located. Without modern simulation tools and experience, there would be a risk of developing a non-functional system. Later troubleshooting can lead to immense costs, delays and even deterioration in a company's image. This is why we always recommend investing sufficient time in reviewing the design even before manufacturing the printed circuit board. The review includes an inspection and simulation of the layout that is as complete as possible in addition to an examination of the entire transmission channel. This means taking into account all of the components, from the signal source to the receiver, and not just the carrier PCB. Satisfactory simulation results for the carrier layout, however, do not guarantee reliable function. The parameters of the actual components can deviate from the values used in the simulation under certain circumstances. This can stem from component tolerances, the production process at the PCB manufacturer or incorrectly simulation parameters. Therefore, a check of the assembled carrier has to be carried out at the end of every carrier development process. In practice, there are often different approaches and levels of testing rigor.

3.6. TEST PROCEDURE

The simplest type of carrier check is a pure function test. In this approach, the COM carrier is equipped with the COM module, function cards, hard drives, etc. Then a test is performed to see whether all system components can be accessed and to check other parameters, such as the transmission rate achieved by the hard drives. These tests are well-suited for initial commissioning

and debugging, but they can only provide very limited useful information for the final verification of a COM carrier. In the event that this sort of test provides a positive result, it is impossible to tell whether there is sufficient safety margin relative to the limit values of the respective bus systems (e.g. jitter) or if the requirements are just barely met. Furthermore, there is a risk that the same set-up will not provide reliable function with different equipment, such as PCIe cards from another manufacturer or from another production batch. This can lead to complex debugging and costly replacement deliveries. For this reason, the function test should be used solely for initial commissioning and debugging but not for final verification of the COM carrier. A reliable inspection of all carrier parameters can be carried out with compliance or precompliance measurements. In these measurements, the quality of the signal is measured, analyzed and compared to specifications of the respective bus. The test is considered to have passed only if all necessary parameters meet the requirements (e.g. total jitter, rise time, fall time, differential skew, spread-spectrum modulation deviation, differential output voltage, eye width, etc.).

3.7. COMPLIANCE/PRECOMPLIANCE MEASUREMENTS

3.7.1. Sequence of compliance/precompliance measurements

The sequence of compliance/precompliance measurements for most modern bus systems is divided into two measurements: Tx measurement and Rx measurement. These are carried out independently of each other. A rough overview of these is provided below.

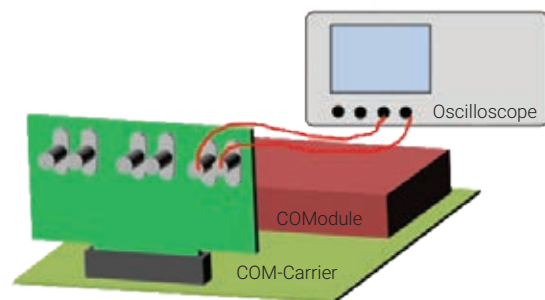


Figure 9: Tx measurement, diagrammatic view

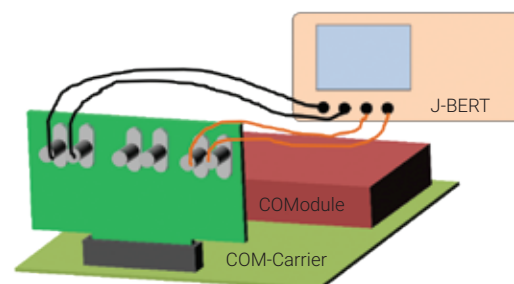


Figure 10: Rx measurement, diagrammatic view

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During Tx measurement, the transmitter on the COM module sends a bit pattern. This bit pattern is measured on a calibrated measurement card using an oscilloscope. The received signal is then examined on an oscilloscope and the individual parameters are compared to the required values from the bus specification.

In an Rx measurement, the data is transmitted from the J-BERT to the receiver on the COM module through the calibrated measurement card. The J-BERT simulates a „stressed eye“ signal that contains defined impairments such as worst eye-opening, maximum permitted jitter and so forth. The COM module receives this data and transmits the same data back to the J-BERT to observe whether the Rx data is detected correctly.

The calibrated measurement cards in use are mandated by the respective bus specification and emulate „real“ peripheral cards for the bus system (e.g. SATA, USB, PCIe, etc.). If the specifications for signal quality are met with these cards, reliable function is assured when using all standard peripheral cards.

3.7.2. Value of compliance/precompliance measurements

Compliance/precompliance measurements, unlike a pure function test, also provide more than just a „PASS/FAIL“ statement. They also demonstrate the quality of the signal for the transmit and receive directions as measured values. These values can be used to check the accuracy of simulations and to readjust the parameters of the simulations if necessary. This leads to more precise information through simulations for future projects. In addition, the measured values show how much reserve is available relative to each limit value and thus how robust the carrier or entire system is in relation to additional interference factors.

4. COOLING DESIGN DEVELOPMENT FOR A COM CARRIER SYSTEM

Due to the continually increasing integration density of electronics and, as a result, higher thermal load per unit of space, the requirements for heat dissipation for electronic components and systems also continue to grow. Therefore, it is essential that the cooling design is integrated into the development process right from the start when developing the COM carrier. Using state-of-the-art simulation methods, a wide range of variants can be validated before detailed development starts.

In the past, an iterative development process in the test lab using prototypes achieved satisfactory cooling results. However, this method is no longer practical due to current requirements for costs and development time (time to market). In particular,

prototypes and samples usually become available only very late in the development process. The risk of changes in later project phases, which may cause delays and high follow-up costs, remains high in comparison. Computational development methods (CAE, Computer Aided Engineering), on the other hand, have made tremendous progress in recent decades with respect to accuracy and user-friendliness. Thanks to the computing capacity of state-of-the-art hardware, these methods have become an efficient tool. However, it requires that the developers make a few simplifications and assumptions due to missing data, leading to the need to validate the simulations through measurements and tests. The number of tests and variants can be significantly reduced, however. This is why a combined method is used for developing the cooling concept of the COM carrier. The system is designed with the aid of thermal simulations. A series of measurements are then performed to validate the calculations.

4.1. COOLING DESIGN – DEVELOPMENT WITH SIMULATIONS

The COM carrier requires that a COM express module is able to dissipate heat up to a power 45 W to the ambient through thermal conduction alone, without the need for forced air flow. In this process, the touchable surface must not have a temperature exceeding 50 °C in order to prevent burn injuries upon contact. In addition, there is increasing demand for easy module replacement, which requires an easy-to-open case with efficient heat sink removal. For this reason, an adapter plate is used (Fig. 11). This plate is permanently connected to the heat spreader of the COM module, sealing the case against the ingress of dirt, water and electromagnetic waves. In addition, the plate establishes the thermal connection of the heat spreader to the heat sink. Thermal gap materials compensate for tolerances and unevenness.



Figure 11: Depiction of the COM carrier system.

- 1: removable heat sink;
- 2: adapter plate;
- 3: removable front and top covers for easy access to the electronics.

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A thermal simulation model is created based on the first models from design engineering. This process entails converting the individual components from the CAD model into corresponding electronic and mechanical components. The appropriate physical properties are then assigned to them. The result of the simulations is a detailed image of the temperatures of the individual components and the predominant flow structures that contribute to component cooling (see Fig. 12).

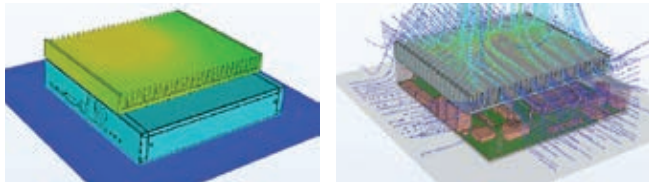


Figure 12: Component temperatures (left) and flow structure (right) as a result of the thermal simulations of the COM carrier system at 1 RU and 250x250 mm

4.2. MEASUREMENT SETUP AND TEST RESULTS

The heat sinks are designed for the carrier system at the beginning of the process with the help of simulations. They are specifically adopted parts. In order to efficiently achieve a wider range of variants for the test series, additional heat sinks from standard profiles are procured from suppliers. Since the COM modules and the positions of the primary heat sources vary on the specific modules, dummy modules with load resistances and heat spreaders are used for the measurements, which allows for easy adjustment of thermal loads.

The components in the thermal conduction path, i.e. modules, heat spreaders, adapter plates and heat sinks, are equipped with temperature sensors at all four corners and on both sides. The sensors are installed in grooves made in the surface and glued in with thermal adhesives to ensure that they do not cause any further unevenness and the heat transfer between the individual surfaces remains unaffected (Fig. 12). The tests are carried out in a climate chamber with the option of air conditioning. In addition, potential interference variables are examined and minimized at the beginning of the test series. Each individual measurement is carried out for as long as it takes to achieve a steady state condition.



Figure 13: COM carrier in the climate chamber equipped with sensors and a Schroff heat sink (left); position of the temperature sensors glued into the grooves (right).

At the beginning of the measurements, it was shown that the thermal mass of the system is very high, such that the measurements must be extended to several hours before the system reaches a steady state. In particular, this is caused by the high thermal storage capacity of the heavy heat sink in comparison to the relatively low power of 45 W introduced into the system.

Furthermore, even small disturbances, such as the entrance of laboratory personnel into the climate chamber, are evident on the measurement curves. Hence, the conditioning system of the climate chamber proves to be a major interference factor. This system uses multiple fans to circulate the chamber air in order to reach an air temperature distribution that is as homogeneous as possible. Air movements caused by this process increase the heat transfer on the system, especially on the heat sink, which results in very low temperatures for the electronic components during conditioned test operation. For this reason, the tests are still carried out in the climate chamber with protection from outside influences, but with the conditioning system switched off. Measured values obtained this way for the cooling system, and for the thermal resistance of the heat sink in particular, lead to a better match with the manufacturer specifications and simulation results.

The measurement results are visualized using the example of two different heat sinks that have significantly different shapes. Firstly, this test setup is expected to result in measured values that differ more drastically, allowing for easy comparison to the simulations. In addition, it allows better observation of how well the simulation tool deals with the unique features of the various components. The flat and wide heat sink from Schroff in-house manufacturing featuring even fins is a production-oriented model that roughly meets the cooling requirements mentioned above. The reference sample is a tall and short element from the market with shaped fins. Based on the manufacturer specifications, it is clear from the start that this model will provide substantially worse cooling performance. However, it is interesting to use this element to learn whether the simulations are able to reproduce the cooling effect of the fins with sufficient accuracy. According to the data sheet from the manufacturer, the heat sink has a thermal resistance of approx. 0.8 K/W, assuming horizontal mounting and free convection.

An initial look at the results (Fig. 14) makes clear that, with the series-oriented heat sink, the surface temperature at the top of the fins is just over the 50 °C requirement at an ambient temperature of 20 °C. This is the same result as inferred from the design calculations. The reference heat sink very clearly exceeds this requirement. The surface temperature at the end of the fins would reach more than 65 °C. It is also important to note here that the thermal resistance of the reference heat sink is slightly higher than the specified value of 0.8 W/K.

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The measurements yielded a resistance of a little more than 0.9 W/K. This is presumably due to the fact that only the surface area of the adapter plate is connected to the heat source instead of the entire bottom side of the heat sink.

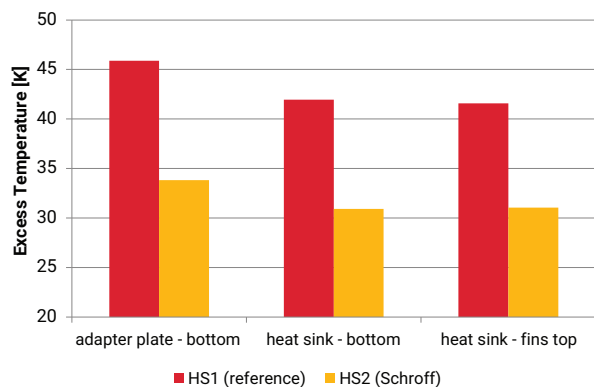


Figure 14: Measurement results for excess temperature (measured temperature relative to the ambient temperature) for the reference sample (KK1) and the series-oriented Schroff heat sink (KK2).

It is interesting to note here that the glass-fiber-reinforced heat conduction foil between the heat sink and the adapter plate leads to differences in temperature reduction between variants. Obviously, it is difficult to consistently guarantee the same thermal performance using the foil. Lower fluctuations can be achieved when softer foils without glass-fiber reinforcement are used. The differences for the reinforced foils, however, are reduced to such a low enough level overall that the advantages in handling outweigh the aforementioned disadvantage.

4.3. COMPARING THE MEASUREMENTS TO THE SIMULATIONS

Fig. 15 shows a comparison of the results from simulations and measurements for the versions described above. It is easy to see that the simulations are capable of reproducing the measurements. This is possible, however, only through appropriate configuration of the material properties in the simulation model. As a result, the simulation model can do more than just reproduce the tendencies accurately with a max. deviation of 1.5 K, which is crucial for variant comparison. It is also capable of calculating the absolute values of the temperatures with sufficient accuracy and with an absolute deviation below 3 K, which corresponds to a relative tolerance of max. 7%. This allows for a precise design of the system to meet specific requirements.

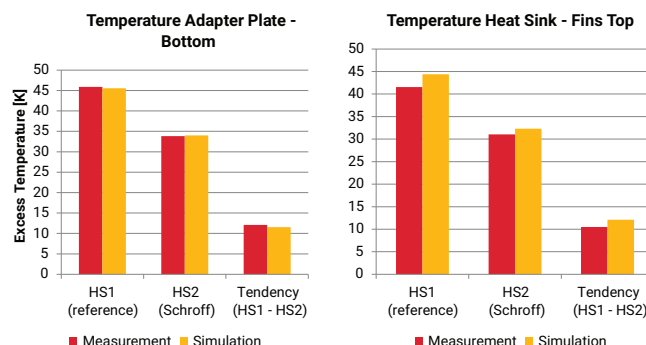


Figure 15: Comparison of measurement and simulation results for both heat sinks, at adapter plate bottom side (left) and heatsink fins (right).

5. SUMMARY

For the enclosure design, it is important to develop a simple solution matched specifically to the application, with the aid of countless modification options. Falling back on an existing enclosure solution that has already been tested for EMC and IP protection is also recommended. Mounting an enclosure using a horizontal rail installation, for example, or installation using a Vesa adapter should also be incorporated into the development process.

In order to ensure the signal integrity and reliability of data transmission, a number of parameters have to be taken into account and fulfilled in the design of the COM carrier printed circuit board from a signal and power integrity perspective. The use of simulation tools is highly recommended and we consider it almost mandatory. The insights from simulations allow optimizations, reduce risks and provide insights for future projects. A final compliance/precompliance measurement that is as comprehensive as possible for the carrier design enables reliable and robust operation of the assembly. It also provides insight into the accuracy of simulations, which is, in turn, important for future projects.

Simulations of the cooling designs subsequently tested through measurements in a climate lab are used to ensure sufficient cooling. Various thermal flow simulations are used in the development process for a COM carrier system for system design in order to optimize passive cooling using heat sinks. The result is a modular system that can be adapted to meet various customer requirements through selection from a series of available heat sinks. Measurements are carried out at a climate lab for comparing the simulation results. Various interference sources are identified and corrected systematically. The goal is for measurement results to verify the simulations and definitively prove the functionality of the cooling design with analysis indicating that there is very close agreement between the measurement results and simulations.

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ABOUT THE AUTHORS

Christian Ganninger, born 1971, studied electrical engineering at the University of Applied Science in Karlsruhe, Germany. Subsequently, he worked as design engineer und technical coordinator backplanes and later as project manager backplanes & systems in a company, which develops and produces 19"-systems and backplanes. Since May 2005 he is Product Manager Backplanes at Schroff GmbH. Later he took over the Product Management for MicroTCA, Power Supplies and Rugged Enhanced Systems too. After one year being Category Manager Systems EMEA in 2011 he took over the Product Management Systems EMEA. Since January 2014 he is Global Product Manager Systems.

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Sergej Dizel, has the role of Principal Engineer for backplanes at Schroff GmbH and is responsible for signal integrity

More information about the COM Carrier here:

<https://schroff.nvent.com/en/schroff/computer-on-modules>

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